

# REALTEK

## ALC5621

### I<sup>2</sup>S AUDIO CODEC + 2.6W CLASS-AB/D MONO SPEAKER AMPLIFIER + HEADPHONE AMPLIFIER

## DATASHEET

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## **USING THIS DOCUMENT**

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5621 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## **REVISION HISTORY**

| <b>Revision</b> | <b>Release Date</b> | <b>Summary</b>                                                                                                                                                                                  |
|-----------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.0             | 2007/12/27          | First release                                                                                                                                                                                   |
| 1.1             | 2008/11/13          | Revised Table 3, page 8.<br>Revised section 10 Application Circuit, page 65.                                                                                                                    |
| 1.2             | 2009/07/21          | Revised Class-AB/D mono speaker amplifier output power.<br>Revised Table 81, page 59.<br>Revised section 10 Application Circuit, page 65.<br>Revised section 11 Mechanical Dimensions, page 66. |

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# 1. General Description

The ALC5621 is a highly-integrated I<sup>2</sup>S/PCM interface audio codec with multiple input/output ports and is designed for mobile computing and communications. It provides a Stereo Hi-Fi DAC for playback and Stereo ADC for recording via the I<sup>2</sup>S/PCM interface.

To reduce component count, the device can connect directly to:

- MONO or stereo differential analog inputs
- LINE\_IN stereo single-ended analog inputs
- AUX\_IN single-ended analog inputs
- Stereo Headphone Output
- Single-ended stereo configurable to AUXOUT or BTL MONO\_OUT
- MONO or Stereo Bridge-Tied Load (BTL) speaker

Multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices. Differential input/output connections efficiently reduce noise interference, providing better sound quality. Class-AB or Class-D amplifiers are easily swapped via simple register configuration, and the 2.6-Watt Mono speaker removes the need for an additional amplifier, further cutting both cost and required board area. Additionally, a flexible hardware 5-band equalizer with configurable gain, bandwidth, and center frequency, enriches the sound experience.

The ALC5621 AVDD operates at supply voltages from 2.3V to 3.6V. DVDD operates from 1.71 to 3.6V, and SPKVDD operates from 2.3 to 5V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10 $\mu$ A.

The ALC5621 is available in a 5x5mm ‘Green’ QFN-32 package, making it ideal for use in handheld portable systems.

## 2. Features

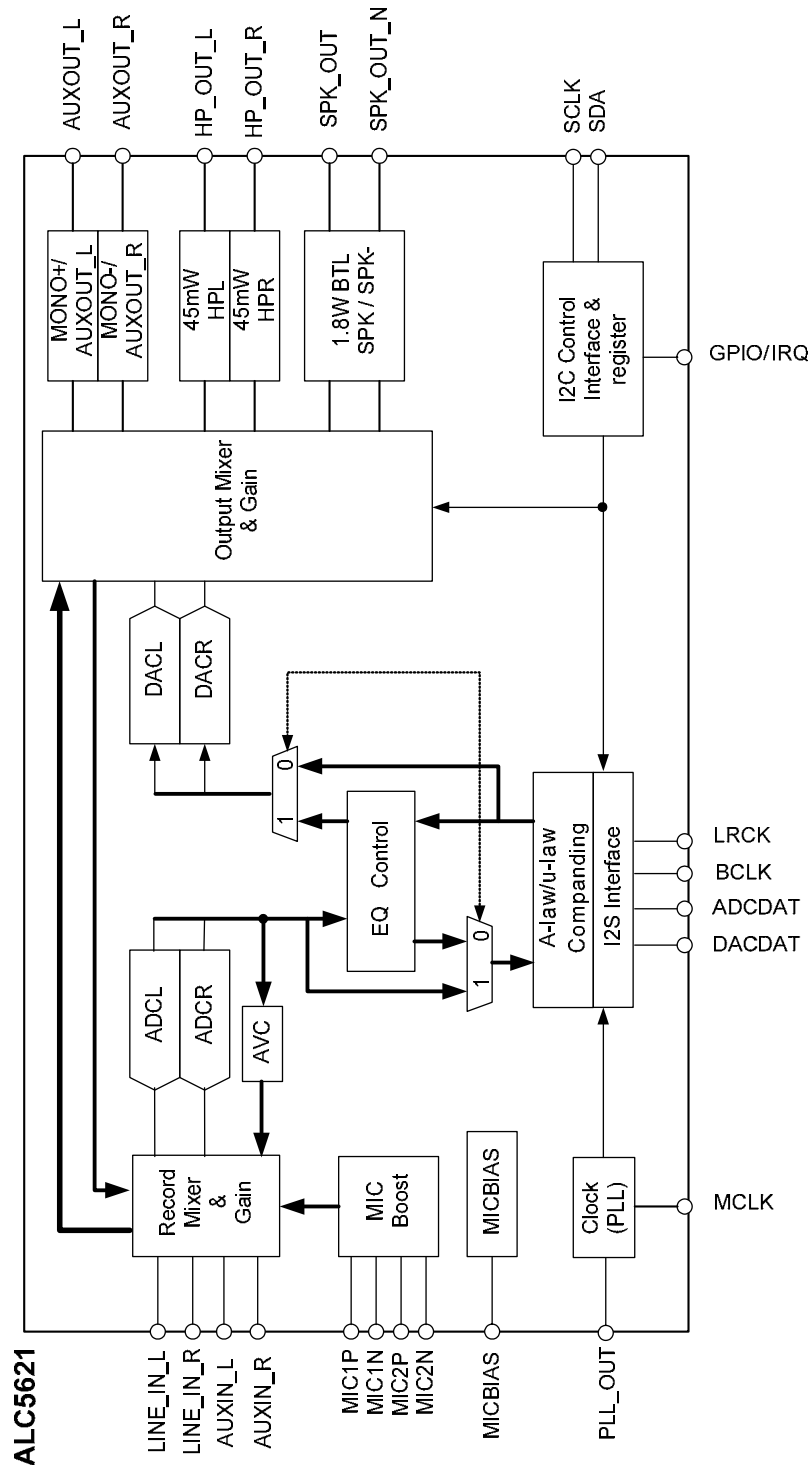
- Digital-to-Analog Converter with 92dB SNR and –85dB THD+N
- Analog-to-Digital Converter with 85dB SNR and –80dB THD+N
- Two analog stereo single-ended inputs, LINE-IN\_L/R and AUXIN\_L/R
- Stereo differential analog microphone inputs, with boost pre-amplifiers (+20/+30)
- BTL (Bridge-Tied Load) Speaker output with on-chip 2.6W speaker driver (SPKVDD=5V, 4Ω load with THD+N=20dB)
- Mono Speaker output supports Class-AB or Class-D optional
- Stereo headphone output with on-chip 45mW headphone driver (AVDD=3.3V, 16Ω load)
- 25mW SE or 75mW BTL single-ended differential MONO\_OUT configurable to AUXOUT (AVDD=3.3V, 32Ω load)
- Audio jack insert detection and microphone switch detection
- Power management and enhanced power saving
- Supports digital 5-band equalizer (EQ)
- Supports digital spatial sound and pseudo stereo effect
- Supports pop noise suppression
- Internal PLL can receive wide range of clock input
- Digital power supplies from 1.71V to 3.6V; speaker amplifier power supplies from 2.3V to 5V
- Analog power and headphone power supplied from 2.3V to 3.6V
- Supports soft-mute function
- 32-pin QFN package

### **3. System Applications**

- Tablet PC system/Ultra-Mobile PC (UMPC)
- Personal Digital Assistants (PDA) or PDA Phone
- Multimedia Phone Applications
- Portable Navigation Device (PND)
- Bluetooth Headphone

## 4. Block Diagrams

### 4.1. Function Block



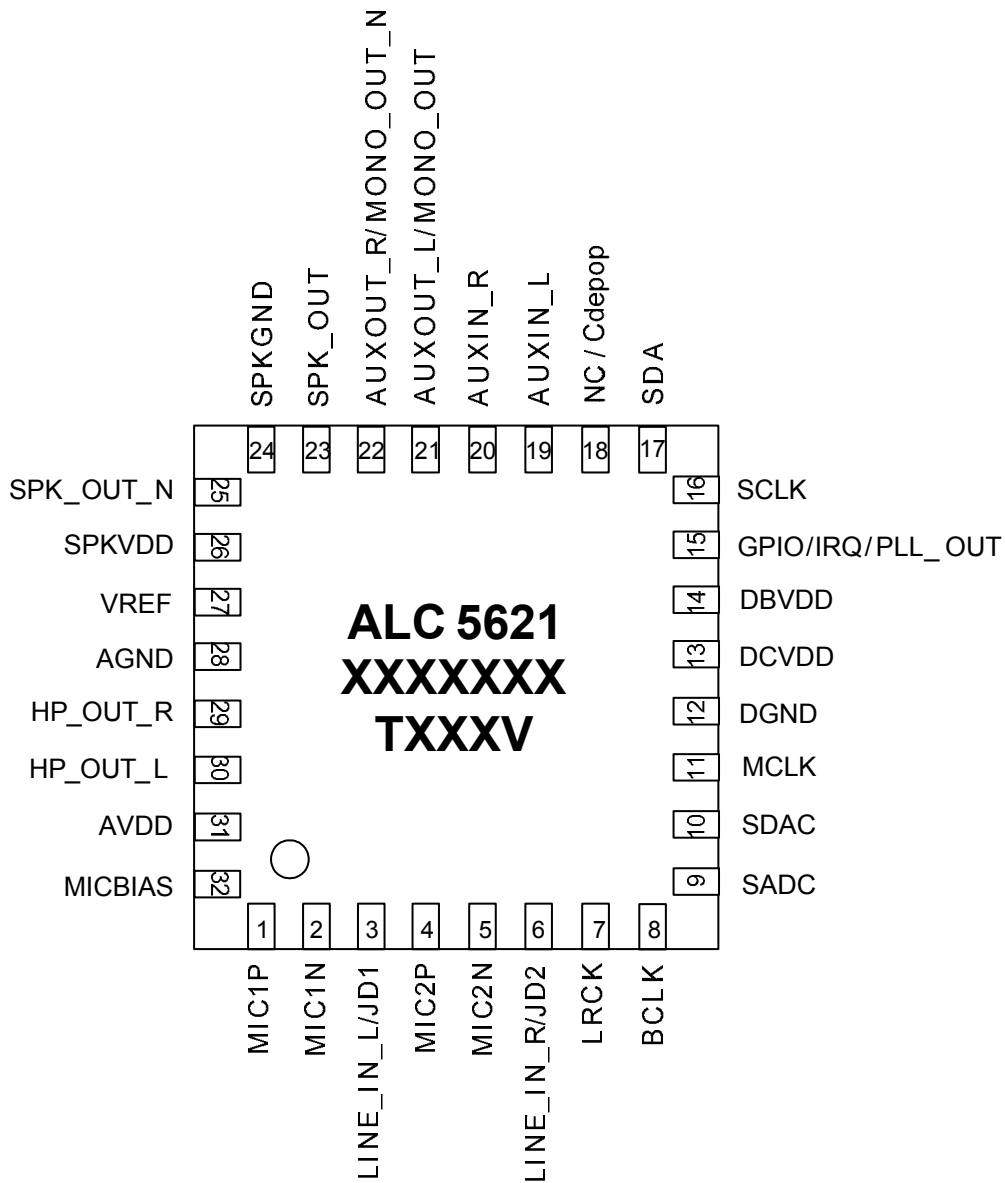
**Figure 1. Block Diagram**

***I<sup>2</sup>S Audio Codec + 2.6W Class-AB/D Mono Speaker Amplifier + Headphone Amplifier*** 5



**Figure 2. Audio Mixer Path**

## 5. Pin Assignments



**Figure 3. Pin Assignments**

### 5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3.

## 6. Pin Descriptions

### 6.1. Digital I/O Pins

**Table 1. Digital I/O Pins**

| Name                     | Type           | Pin | Description                                                          | Characteristic Definition                                                       |
|--------------------------|----------------|-----|----------------------------------------------------------------------|---------------------------------------------------------------------------------|
| LRCK                     | IO             | 7   | Digital Audio Synchronous Signal                                     | Master: $V_{OL} = 0.1 * DVDD$ , $V_{OH} = 0.9 * DVDD$<br>Slave: Schmitt trigger |
| BCLK                     | IO             | 8   | Digital Audio Serial Clock                                           | Master: $V_{OL} = 0.1 * DVDD$ , $V_{OH} = 0.9 * DVDD$<br>Slave: Schmitt trigger |
| SADC                     | O              | 9   | Serial ADC Data Output                                               | $V_{OL} = 0.1 * DVDD$ , $V_{OH} = 0.9 * DVDD$                                   |
| SDAC                     | I              | 10  | Serial DAC Data Input                                                | Schmitt trigger                                                                 |
| MCLK                     | I              | 11  | Master Clock Input                                                   | Schmitt trigger                                                                 |
| GPIO/<br>IRQ/<br>PLL_OUT | IO/<br>O/<br>O | 15  | General Purpose Input And Output/<br>Interrupt Output/<br>PLL Output | GPIO: Input/Output<br>IRQOUT: Output<br>PLL_OUT: Output                         |
| SCLK                     | I              | 16  | I <sup>2</sup> C Clock                                               | Schmitt trigger                                                                 |
| SDA                      | IO             | 17  | I <sup>2</sup> C Data                                                | Schmitt trigger                                                                 |
|                          |                |     |                                                                      | Total: 8 Pins                                                                   |

### 6.2. Analog I/O Pins

**Table 2. Analog I/O Pins**

| Name                    | Type | Pin | Description                                         | Characteristic Definition          |
|-------------------------|------|-----|-----------------------------------------------------|------------------------------------|
| MIC1P                   | I    | 1   | First Mic Positive Input                            | Analog Input (1Vrms)               |
| MIC1N                   | I    | 2   | First Mic Negative Input                            | Analog Input (1Vrms)               |
| LINE_IN_L/JD1           | I    | 3   | Line Input Left Channel/Jack Detect Input_1         | Analog Input (1Vrms)               |
| MIC2P                   | I    | 4   | Second Mic Positive Input                           | Analog Input (1Vrms)               |
| MIC2N                   | I    | 5   | Second Mic Negative Input                           | Analog Input (1Vrms)               |
| LINE_IN_R/JD2           | I    | 6   | Line Input Right Channel/Jack Detect Input_2        | Analog Input (1Vrms)               |
| AUXIN_L                 | I    | 19  | Auxiliary Input Left Channel                        | Analog Input (1Vrms)               |
| AUXIN_R                 | I    | 20  | Auxiliary Input Right Channel                       | Analog Input (1Vrms)               |
| AUXOUT_L/<br>MONO_OUT   | O    | 21  | Positive Mono Output/Auxiliary Output Left Channel  | Analog Output (1Vrms)              |
| AUXOUT_R/<br>MONO_OUT_N | O    | 22  | Negative Mono Output/Auxiliary Output Right Channel | Analog Output (1Vrms)              |
| SPK_OUT                 | O    | 23  | Speaker Output                                      | Analog Output (1.5Vrms, SPKVDD=5V) |
| SPK_OUT_N               | O    | 25  | Negative Speaker Output                             | Analog Output (1.5Vrms, SPKVDD=5V) |
| HP_OUT_R                | O    | 29  | Headphone Output Right Channel                      | Analog Output (1Vrms)              |
| HP_OUT_L                | O    | 30  | Headphone Output Left Channel                       | Analog Output (1Vrms)              |
|                         |      |     |                                                     | Total: 14 Pins                     |

### 6.3. Filter/Reference

**Table 3. Filter/Reference**

| Name      | Type | Pin | Description                | Characteristic Definition                    |
|-----------|------|-----|----------------------------|----------------------------------------------|
| NC/Cdepop | IO   | 18  | NC/De-Pop Capacitor        | 0.1 $\mu$ f capacitor to analog ground       |
| VREF      | O    | 27  | Internal Reference Voltage | 4.7 $\mu$ f capacitor to analog ground       |
| MICBIAS   | O    | 32  | MIC BIAS Voltage Output    | Programmable Analog DC output with 3mA drive |
|           |      |     |                            | Total: 3 Pins                                |

### 6.4. Power/Ground

**Table 4. Power/Ground**

| Name   | Type | Pin         | Description                                                  | Characteristic Definition |
|--------|------|-------------|--------------------------------------------------------------|---------------------------|
| DGND   | P    | 12          | Digital GND                                                  | -                         |
| DCVDD  | P    | 13          | Digital VDD                                                  | 1.71V~3.6V (Core)         |
| DBVDD  | P    | 14          | Digital VDD                                                  | 1.71V~3.6V (IO Buffer)    |
| SPKGND | P    | 24          | Analog GND for Speaker Amps                                  | -                         |
| SPKVDD | P    | 26          | Analog VDD for Speaker Amps                                  | 2.3V~5V                   |
| AGND   | P    | 28          | Analog GND                                                   | -                         |
| AVDD   | P    | 31          | Analog VDD                                                   | 2.3V~3.6V                 |
| SPKGND | P    | Exposed Pad | Speaker amplifier GND<br>Must be connected to system<br>DGND | -                         |
|        |      |             |                                                              | Total: 8 Pins             |

Note:  $DBVDD \geq DCVDD$ .  $SPKVDD \geq AVDD \geq DCVDD$ .

## 7. Functional Description

### 7.1. Power

The ALC5621 has many power blocks. SPKVDD operates between 2.3V and 3.0V for weak Class-AB amplifiers, and between 3V and 5V for strong Class-AB amplifiers. The full range is available for Class-D amplifiers.

AVDD operates between 2.3V and 3.6V. DBVDD and DCVDD operate between 1.71V and 3.6V. The ALC5621 must handle ratio control between the different power blocks. The power supplier limit conditions are  $DBVDD \geq DCVDD$ , and  $SPKVDD \geq AVDD \geq DCVDD$ .

### 7.2. Reset

There are two types of reset operation: Power-On Reset (POR) and Register reset.

**Table 5. Reset Operation**

| Reset Type     | Trigger Condition                                    | CODEC Response                                                    |
|----------------|------------------------------------------------------|-------------------------------------------------------------------|
| POR            | Monitor digital power supply voltage reach $V_{POR}$ | Reset all hardware logic and all registers to default values.     |
| Register Reset | Write Reg-00h                                        | Reset all registers to default values except PLL related register |

#### 7.2.1. Power-On Reset (POR)

When powered on, DCVDD passes through the  $V_{POR}$  band of ALC5621 ( $V_{PORH} \sim V_{PORL}$ ). A Power-On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

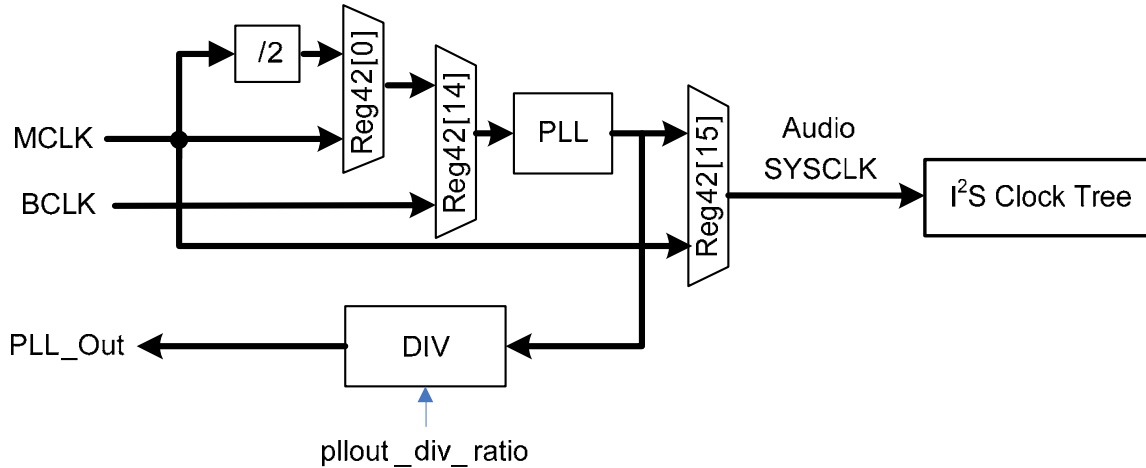
**Table 6. Power-On Reset Voltage**

| Symbol         | Min | Typical | Max | Unit |
|----------------|-----|---------|-----|------|
| $V_{POR\_ON}$  | 1.0 | -       | 1.6 | V    |
| $V_{POR\_OFF}$ | -   | 1.3     | -   | V    |

Note:  $V_{POR\_OFF}$  must be below  $V_{POR\_ON}$ .

### 7.3. Clocking

The Audio SYSCLK can be selected from MCLK or PLL. The clock source of PLL can be selected from MCLK or BCLK. The ALC5621 only supports 256Fs or 384Fs as Audio SYSCLK (used as Stereo I<sup>2</sup>S clock).



**Figure 4. Audio SYSCLK**

#### 7.3.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. Typical choices are 2.048MHz, 4.096MHz, and 13MHz. The source of the PLL can be set to MCLK or BCLK by setting pll\_sour\_sel (Reg42[14]).

The source clock of MCLK must be able to drive I<sup>2</sup>C, and F/W can setup PLL to output the desired frequency as the SYSCLK.

The PLL transmit formula is:  $F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2))$  {Typical K=2}

**Table 7. Clock Setting Table for 48K (Unit: MHz)**

| MCLK   | N  | M  | F <sub>VCO</sub> | K | F <sub>OUT</sub> |
|--------|----|----|------------------|---|------------------|
| 13     | 66 | 7  | 98.222           | 2 | 24.555           |
| 3.6864 | 78 | 1  | 98.304           | 2 | 24.576           |
| 2.048  | 94 | 0  | 98.304           | 2 | 24.576           |
| 4.096  | 70 | 1  | 98.304           | 2 | 24.576           |
| 12     | 80 | 8  | 98.4             | 2 | 24.6             |
| 15.36  | 81 | 11 | 98.068           | 2 | 24.517           |
| 16     | 78 | 11 | 98.462           | 2 | 24.615           |
| 19.2   | 80 | 14 | 98.4             | 2 | 24.6             |
| 19.68  | 78 | 14 | 98.4             | 2 | 24.6             |

**Table 8. Clock Setting Table for 44.1K (Unit: MHz)**

| MCLK   | N  | M  | F <sub>VCO</sub> | K | F <sub>OUT</sub> |
|--------|----|----|------------------|---|------------------|
| 13     | 68 | 8  | 91               | 2 | 22.75            |
| 3.6864 | 72 | 1  | 90.931           | 2 | 22.733           |
| 2.048  | 86 | 0  | 90.112           | 2 | 22.528           |
| 4.096  | 64 | 1  | 90.112           | 2 | 22.528           |
| 12     | 66 | 7  | 90.667           | 2 | 22.667           |
| 15.36  | 63 | 9  | 90.764           | 2 | 22.691           |
| 16     | 66 | 10 | 90.667           | 2 | 22.667           |
| 19.2   | 64 | 12 | 90.514           | 2 | 22.629           |
| 19.68  | 67 | 13 | 90.528           | 2 | 22.632           |

After a Cold Reset, PLL related Registers are reset to default values, however, they are not reset to default values after a soft-reset (write Reg00).

### 7.3.2. I<sup>2</sup>S Stereo Data Interface

The ALC5621 supports the I<sup>2</sup>S digital interface for Stereo Audio. The stereo audio digital interface is used to input data to the stereo DAC or output data from the stereo ADC. The Stereo Audio Digital Interface can be configured as Master mode or Slave mode. For the Stereo I<sup>2</sup>S Interface, the source system clock is always input from MCLK. Refer to section 12 Appendix A: Stereo I<sup>2</sup>S Clock Table, page 67 for details.

#### Master Mode

In master mode (stereo\_i2s\_mode\_sel=0), BCLK and LRCK are configured as output. When sel\_sysclk=0, MCLK is used as Stereo SYSCLK. When PLL is enabled and sel\_sysclk=1, MCLK is suggested to provide frequencies shown in Table 7 Clock Setting Table for 48K (Unit: MHz) and Table 8 Clock Setting Table for 44.1K (Unit: MHz). PLL can be configured to support 44.1K and 48K base sampling rate.

#### Slave Mode

In slave mode (stereo\_i2s\_mode\_sel=1), BCLK/LRCK is configured as input. MCLK should provide the BCLK synchronized clock externally as the Stereo\_SYSCLK.

*Note: The ALC5621 does not support different sample rates between SDAC and ADC in Stereo\_I2S/PCM.*

## 7.4. Digital Data Interface

### 7.4.1. Stereo I<sup>2</sup>S/PCM Interface

The stereo I<sup>2</sup>S/PCM interface can be configured as Master mode or Slave mode. Four audio data formats are supported:

- PCM mode
- Left justified mode
- Right justified mode
- I<sup>2</sup>S mode

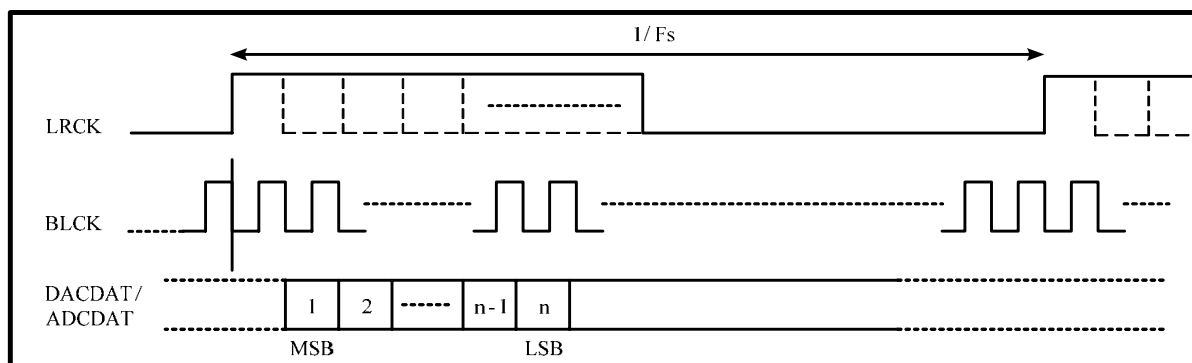


Figure 5. PCM Mono Data Mode A Format (stereo\_i2s\_bclk\_polarity\_ctrl=0, pcm\_mode\_sel=0)

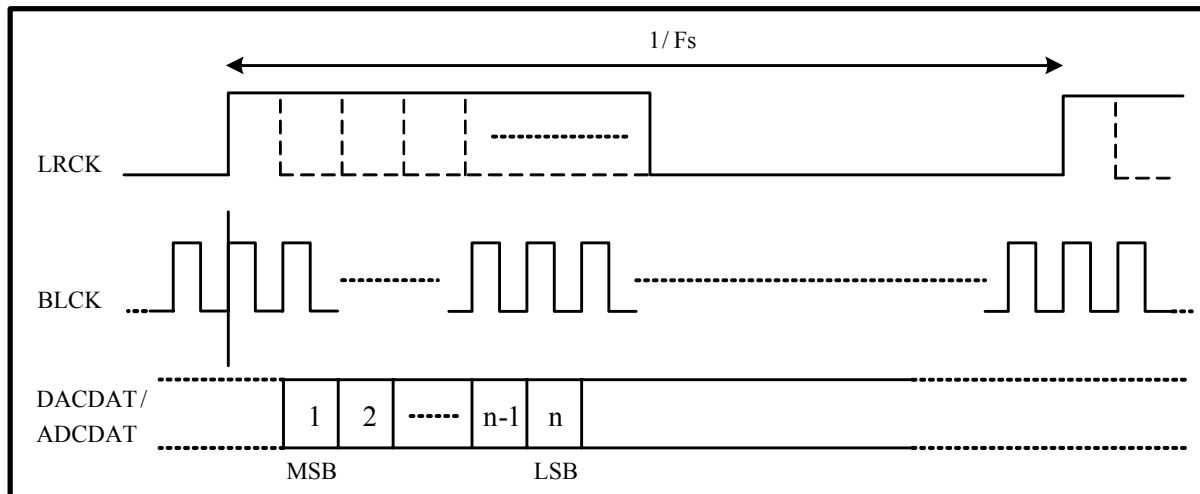
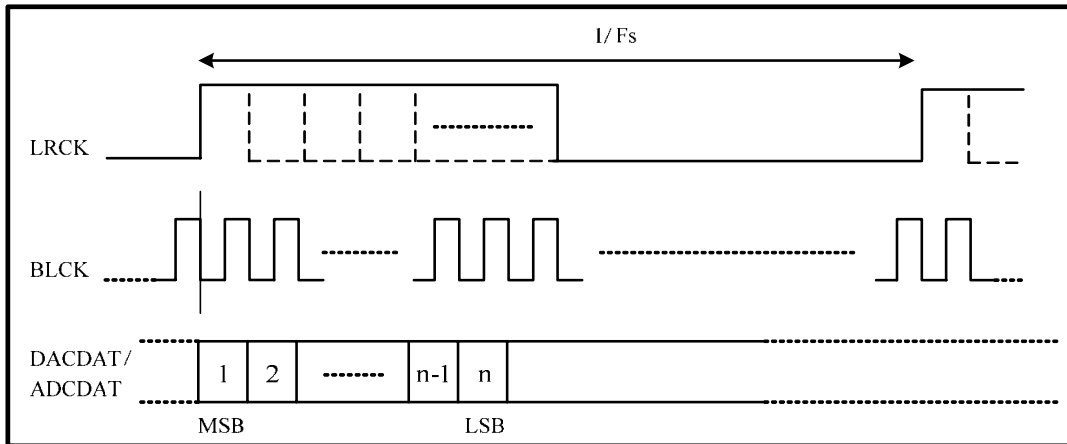
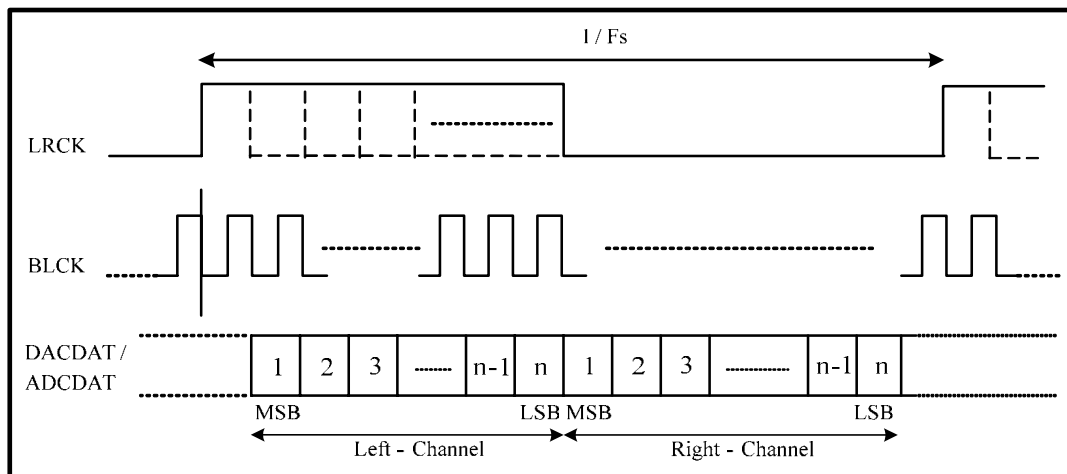


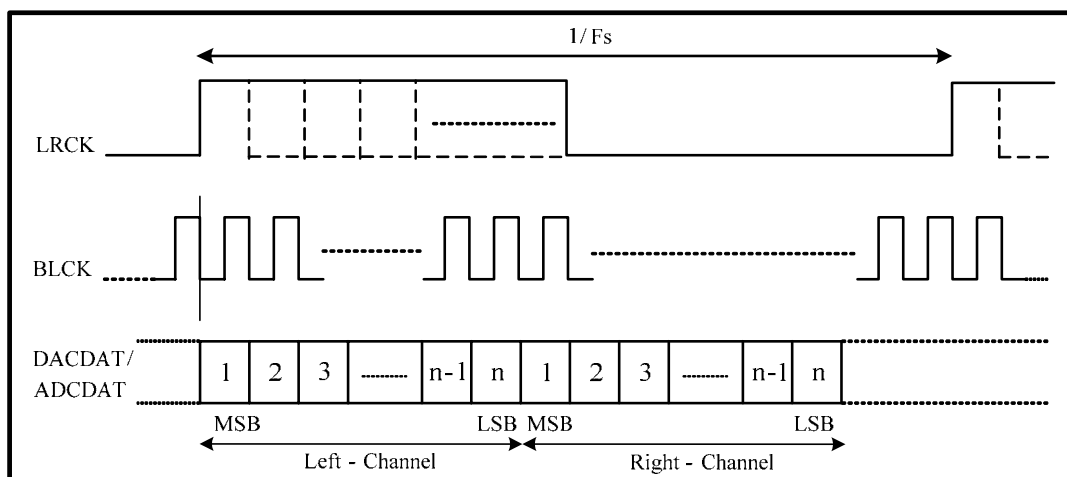
Figure 6. PCM Mono Data Mode A Format (stereo\_i2s\_bclk\_polarity\_ctrl=1, pcm\_mode\_sel=0)



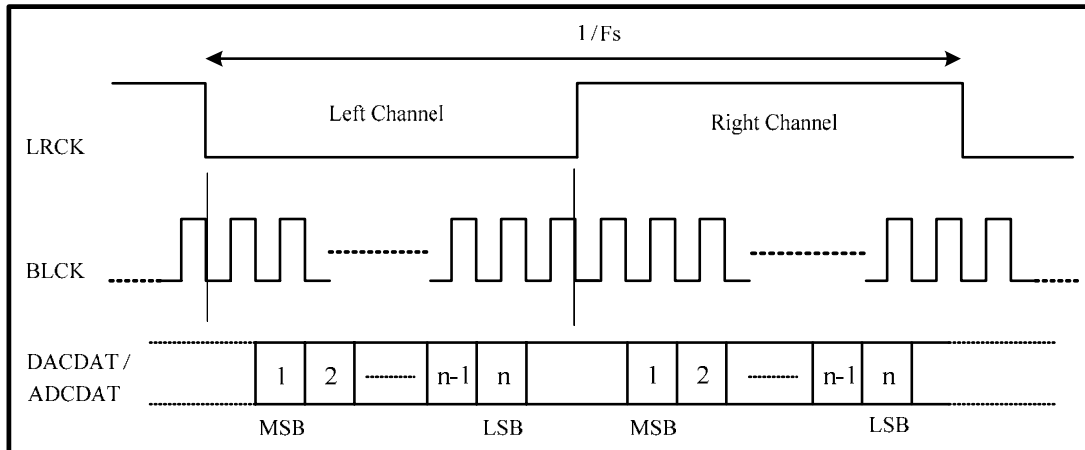
**Figure 7. PCM Mono Data Mode B Format (stereo\_i2s\_bclk\_polarity\_ctrl=0, pcm\_mode\_sel=1)**



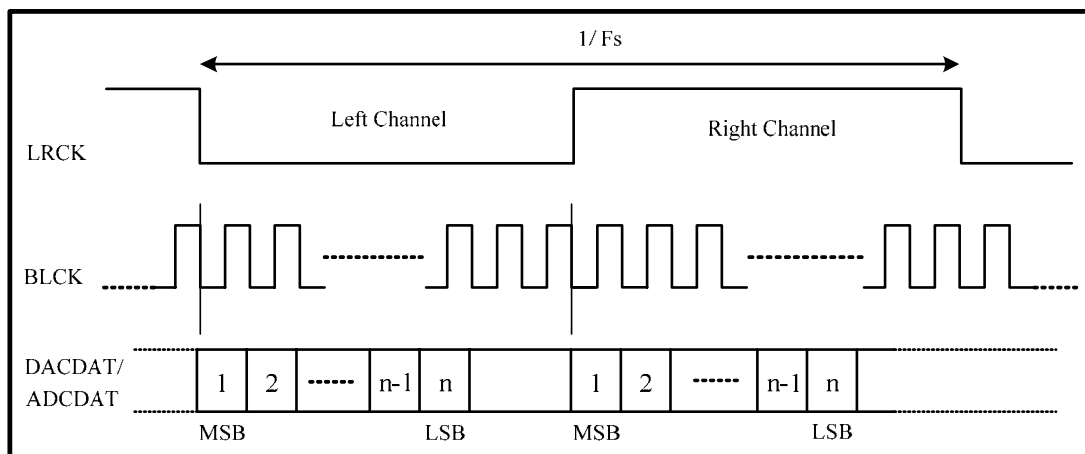
**Figure 8. PCM Stereo Data Mode A Format (stereo\_i2s\_bclk\_polarity\_ctrl=0, pcm\_mode\_sel=0)**



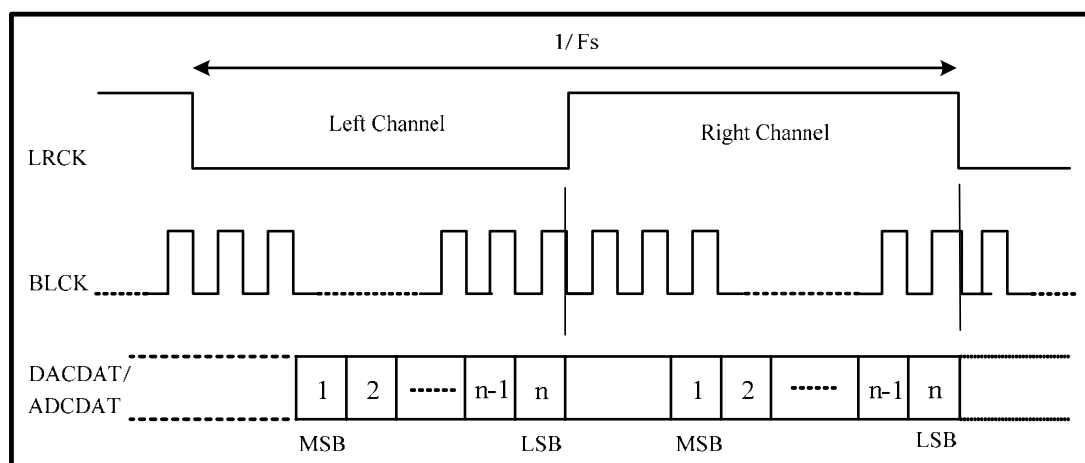
**Figure 9. PCM Stereo Data Mode B Format (stereo\_i2s\_bclk\_polarity\_ctrl=0, pcm\_mode\_sel=1)**



**Figure 10. I<sup>2</sup>S Data Format (stereo\_i2s\_bclk\_polarity\_ctrl=0)**



**Figure 11. Left Justified Data Format (stereo\_i2s\_bclk\_polarity\_ctrl=0)**



**Figure 12. Right Justified Data Format (stereo\_i2s\_bclk\_polarity\_ctrl=0)**

## **7.5. Audio Data Path**

### **7.5.1. Vref**

Vref is the reference voltage for all analog blocks. An external 1 $\mu$ F Capacitor connected to AGND is required. The default status of Vref is enabled after power on. Driver can set Index-39[11]=0b in order to enable power control bit of Reg-3C[13]:pow\_vref.

### **7.5.2. Stereo ADC**

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC is independent of the stereo DAC sample rate. In order to save power, the left and right ADC can be powered down separately by setting adc\_l\_vol & adc\_r\_vol

The sample rate of the Stereo ADC is the same as the sample rate of Stereo DAC (described in the following section).

### **7.5.3. Stereo DAC**

The stereo DAC can be configured to different sample rates by driving 256Fs/384Fs into audio SYSCLK with setting divider properly (Reg36). adda\_osr is used to control the over sample rate clock divider of the DA filter to 128Fs or 64Fs.

Performance of 128Fs is better than 64Fs but with much higher power consumption. Refer to section 12 Appendix A: Stereo I<sup>2</sup>S Clock Table, page 67 for detailed settings.

dac\_l\_vol & dac\_r\_vol can be used to control the DAC output volume.

## **7.6. Mixers**

The ALC5621 supports four mixers for all audio function requirements:

- Headphone mixer for 2 channels
- MONO mixer
- Speaker mixer
- ADC record mixer

### **7.6.1. Headphone Mixer**

The headphone mixer is used to drive stereo output, including HP\_OUT\_L/R, SPK\_OUT, and MONO\_OUT (AUXOUT\_L/R). The output of the headphone mixer can be input to the ADC record mixer.

The following signals can be mixed into the headphone mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- AUXIN\_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

When the SPK\_OUT source is from the HP\_mixer, SPK\_OUT can be configured to L/R, L+R, and L/LN by setting spk\_outn\_source. The HP mixer can be powered down by setting pow\_mix\_hp\_l & pow\_mix\_hp\_r.

### **7.6.2. MONO Mixer**

The MONO mixer is used to drive MONO\_OUT (AUXOUT\_L/R) and SPK\_OUT. The output of the MONO mixer can be input to the ADC record mixer. The output of the MONO mixer is two channels with the same signal.

The following signals can be mixed into the MONO mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- AUXIN\_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)

- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

*Note: The MONO mixer can be powered down by setting `pow_mix_mono`.*

### 7.6.3. Speaker Mixer

The speaker mixer is the same as the MONO mixer and is used to drive MONO\_OUT(AUXOUT\_L/R) and SPK\_OUT. The output of the speaker mixer can be input to the ADC record mixer. The output of the speaker mixer is two channels with the same signal.

The following signals can be mixed into the speaker mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- AUXIN\_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)

*Note: The speaker mixer can be powered down by setting `pow_mix_spk`.*

### 7.6.4. ADC Record Mixer

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. Output of the ADC record mixer can be input to the headphone mixer, MONO mixer, and speaker mixer.

The following signals can be mixed into the ADC record mixer:

- LINE-IN\_L/R (Controlled by Reg0A)
- AUXIN\_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22)
- Headphone mixer output
- MONO mixer output
- Speaker mixer output

*Note: The ADC record mixer can be powered down by setting `pow_mix_adc_rec_l` & `pow_mix_adc_rec_r`.*

## **7.7. Analog Audio Input Path**

The ALC5621 supports four Analog Audio Input paths:

- Line\_IN\_L/R
- AUXIN\_L/R
- MIC1
- MIC2

### **7.7.1. Line Input**

LINE\_IN\_L and LINE\_IN\_R provide 2-channel stereo single-ended input that can be mixed into any analog output mixer and ADC record mixer.

The LINE\_IN\_L/R volume and mute are controlled by Reg0A.  
pow\_li\_l\_vol and pow\_li\_r\_vol can be used to power down LINE\_IN volume control.

LINE\_IN\_L is pin shared to JD1 and can be configured by lineinl\_pin\_sharing.  
LINE\_IN\_R is pin shared to JD2 and can be configured by lineinr\_pin\_sharing.

### **7.7.2. AUXiliary Input**

AUXIN\_L and AUXIN\_R provide 2-channel stereo single-ended input that can be mixed into the ADC record mixer and any analog output mixer.

The AUXIN\_L/R volume and mute are controlled by Reg08.  
pow\_auxin\_l\_vol and pow\_auxin\_r\_vol can be used to power down AUXIN\_L/R volume control.

### **7.7.3. Microphone Input**

MIC1P/N and MIC2P/N provide 2-channel stereo differential or single-ended input, via mic1\_diff\_ctrl and mic2\_diff\_ctrl, that can be mixed into the ADC record mixer, or any analog output mixer. MIC1P and MIC2P are main inputs when differential mode is disabled.

The ALC5621 microphone input boost provides 20/30dB boost, set by mic1\_boost\_ctrl (for MIC1) and mic2\_boost\_ctrl (for MIC2). The MIC1/2 volume and mute are controlled by Reg0E.

pow\_mic1\_vol & pow\_mic2\_vol can be used to power down the MIC1/2 volume control path.  
pow\_mic1\_admixer & pow\_mic2\_admixer can be used to power down the MIC1/2 admixer path.

## **7.8. Analog Audio Output Data Path**

The ALC5621 supports three Analog Audio output paths:

- SPK\_OUT\_L/R
- HP\_OUT\_L/R
- MONO\_OUT(AUX\_OUT\_L/R).

### **7.8.1. Speaker Output**

SPK\_OUT\_L/R provides mono differential output and can be configured to dual single-ended output

The SPK\_OUT source is selected in spk\_vol\_in\_sel. Sources are shown below:

- Vmid
- Headphone left mixer
- Speaker mixer
- MONO mixer

The Speaker-out of the ALC5621 supports Class-AB and Class-D type amplifiers and can be selected at spk\_out\_type\_sel. If a Class-D amplifier is selected, the driver must set Index-46=CF00'h. As the power voltage of SPKVDD is usually higher than AVDD, the ALC5621 must set Class-AB Vmid ratio at spk\_ampAB\_ctrl (Reg40[14:12]) and Class-D Vmid ratio at spk\_ampD\_ctrl (Reg40[11:10]) in order to extend the output level.

The SPK\_OUT volume and mute are controlled by Reg02. Also, Reg3E[12]: pow\_spk can be used to power down SPK output. pow\_clsab (Reg3C[15]) is used to power down the Class-AB Amplifier and pow\_clsd (Reg3C[14]) is used to power down the Class-D Amplifier.

SPK\_OUT supports a soft-mute function and a zero cross detect function. The soft-mute function is enabled by sp\_l\_softmute\_en/sp\_r\_softmute\_en, and the zero cross detect function is enabled by sp\_l\_dezero/sp\_r\_dezero.

If spk\_vol\_in\_sel=10b or 11b, SPK\_OUT is configured to differential, only sp\_l\_softmute\_en and sp\_l\_dezero can be used to control the soft-mute and zero cross of SPK\_OUT.

## 7.8.2. Headphone Output

HP\_OUT\_L/R provides stereo single-ended output. The source of HP\_OUT\_L/R can be selected from hp\_l\_in\_sel & hp\_r\_in\_sel (Reg1C[9:8]).

- Vmid
- Headphone mixer

The HP\_OUT\_L/R volume and mute are controlled by Reg04.

pow\_hp\_l\_vol (Reg3E[10]) and pow\_hp\_r\_vol (Reg3E[9]) can be used to power down the HP output volume

HP\_OUT supports soft-mute and zero cross detect function, which can be individually enabled at hp\_l\_softmute\_en/ hp\_r\_softmute\_en and hp\_l\_dezero/ hp\_r\_dezero

## 7.8.3. MONO Output

MONO\_OUT provides one-channel differential MONO\_OUT or stereo single-ended AUXOUT\_L/R via se\_diff\_auxout.

The MONO/AUXOUT source can be selected from Reg1C[7:6], mono\_in\_sel.  
Sources are shown below.

- Vmid
- Headphone mixer (L+R)
- Speaker mixer
- MONO mixer

The MONO/AUXOUT output signal depends on the setting of se\_diff\_auxout & mono\_in\_sel.

**Table 9. MONO/AUXOUT Output Signal Table**

| mono_in_sel         | se_diff_auxout    | MONO/AUXOUT Output Signal |
|---------------------|-------------------|---------------------------|
| Vmid                | Differential Mode | Vmid                      |
|                     | Single-Ended Mode | Vmid                      |
| HP mixer (L/R)      | Differential Mode | L/LN                      |
|                     | Single-Ended Mode | L/R                       |
| Speaker mixer (L+R) | Differential Mode | (L+R)/(L+R)N              |
|                     | Single-Ended Mode | (L+R)/(L+R)               |
| MONO mixer          | Differential Mode | (L+R)/(L+R)N              |
|                     | Single-Ended Mode | (L+R)/(L+R)               |

MONO/AUXOUT volume and mute are controlled by Reg08.

pow\_aux\_outl\_vol (Reg3E[14]) and pow\_aux\_outr\_vol (Reg3E[13]) can be used to power down the volume of MONO/AUXOUT.

If MONO/AUXOUT is configured to stereo single-ended AUXOUT, the soft-mute and zero cross detect function of MONO/AUXOUT can be enabled at AUXO\_l\_softmute\_en/AUXO\_r\_softmute\_en and AUXO\_l\_dezero/AUXO\_r\_dezero.

If MONO/AUX is configured to mono differential MONO\_OUT, only AUXO\_l\_softmute\_en and AUXO\_l\_dezero can be used to control soft-mute and zero cross of MONO/AUXOUT.

## **7.9. *AVC Control***

The Automatic Volume Control (AVC) function dynamically adjusts the input signal quantized by the ADC to an expected sound level by setting THmax, THmin, and THnonact (see Figure 14 AVC Behavior, page 22).

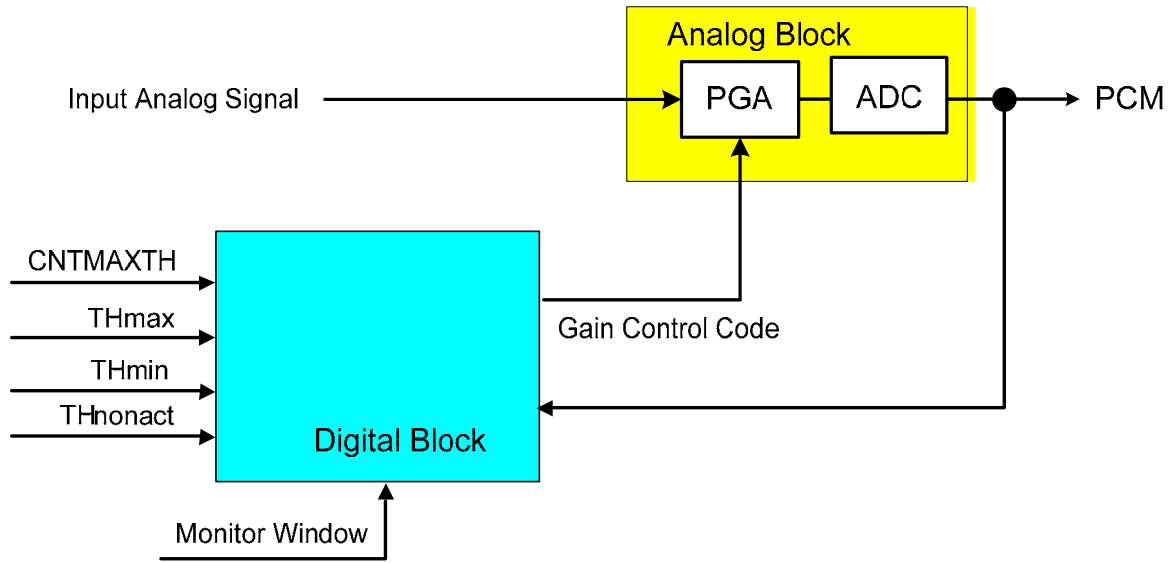
When the average level of input signal is higher than THmax, the AVC will decrease the selected analog gain to attenuate the quantized Pulse Code Modulation (PCM) signal to a lower amplitude than THmax.

When the average level of input signal is lower than THmin and higher than Thnonact., the AVC will increase the selected analog gain to amplify the input signal. The quantized Pulse Code Modulation (PCM) signal is then set to a higher amplitude than THmin. The quantized PCM has an average level between THmin and THmax.

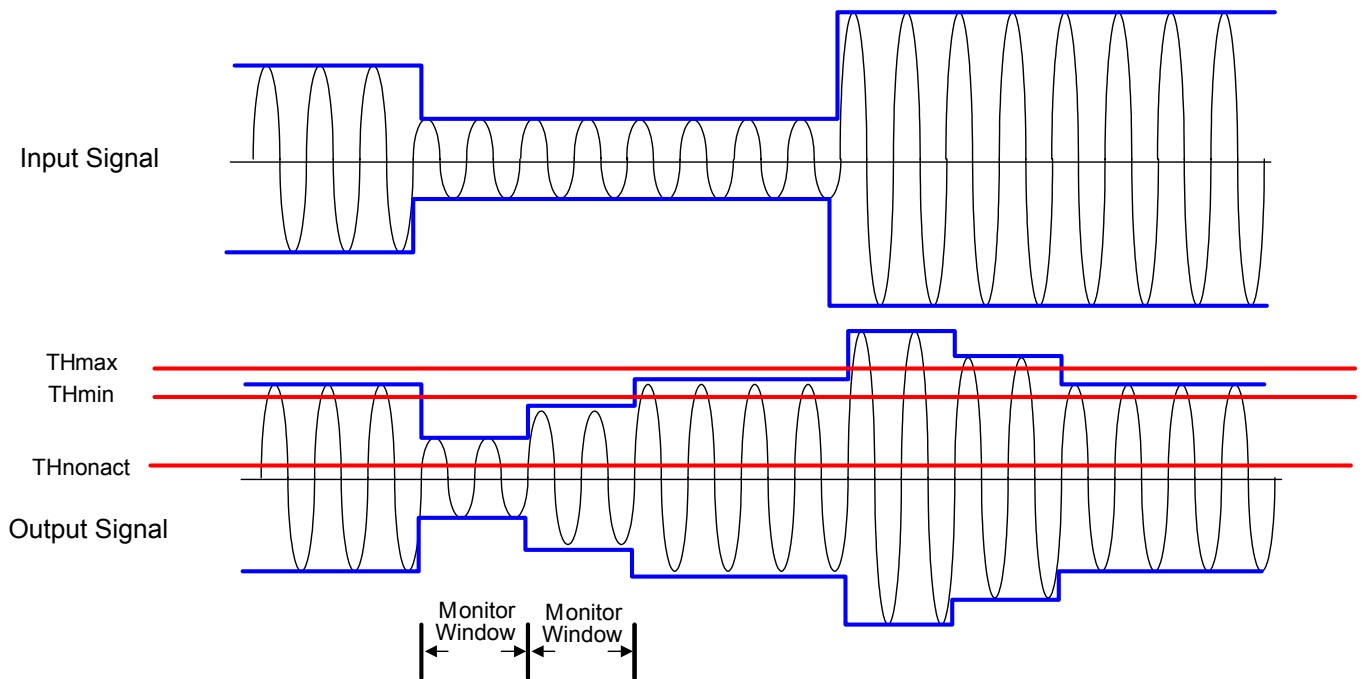
In order not to output a strong amplified signal when the gain detector input level is transiting from a very small signal to a normal signal, the AVC block will limit the selected analog gain to unit gain (=0dB) when the input level of the gain detector is lower than THnonact.

The AVC reference source channel and target channel can be individually set by Reg68: AVC Control.

The AVC block diagram and behavior is shown in Figure 13 and Figure 14, respectively.



**Figure 13. Auto Volume Control Block Diagram**



**Figure 14. AVC Behavior**

## **7.10. Hardware Sound Effects**

The Sound Effect block is composed of Pseudo Stereo, Spatial 3D, and Equalizer blocks. The Pseudo Stereo block is used to convert a MONO source into virtualized stereo output. The Spatial 3D block is a surround sound generator with adjustable amplitude (Gain) and surround depth (Ratio). The Equalizer block can be used to compensate for speaker response, or to make environment sound effects, e.g., 'Pub', 'Live', 'Rock',... etc..

### **7.10.1. Equalizer Block**

The Equalizer block cascades 5 bands of equalizer to compensate for speaker response and to emulate environment sound. One high-pass filter cascaded in the front end is used to drop low frequency tone, which has a larger amplitude and may damage a mini speaker.

The high-pass filter can also be used to adjust Treble strength with gain control. A low-pass filter with gain control can adjust the Bass strength. Three bands of bi-quad bandpass filters are used to emulate environment sounds.

To avoid PCM sample saturation, a digital volume control has 0 ~18dB attenuation in the front of equalizer is required. A -3~+18dB digital gain control after equalizer is used to compensate PCM output to suitable level.

The Equalizer source of the ALC5621 can be selected from DAC or ADC. If Equalizer parameters will be dynamically changed, the driver should set EQ Mode Change enable and disable after the EQ parameters have been set to new values.

### **7.10.2. Pseudo Stereo and Spatial 3D Sound**

There are two spatial effects in post-processing; the Pseudo-Stereo Effect + Spatial Effect, and the Stereo Expansion Effect. The Pseudo-Stereo Effect + Spatial Effect converts a MONO signal to a stereo signal by changing the phase and amplitude of the original signal followed by enhancing the spatial effect. The Stereo Expansion Effect enhances the spatial effect when the input signal is Stereo.

## 7.11. I<sup>2</sup>C Control Interface

I<sup>2</sup>C is a 2-wire half-duplex serial communication interface, supporting only slave mode. The host must support MCLK during register access.

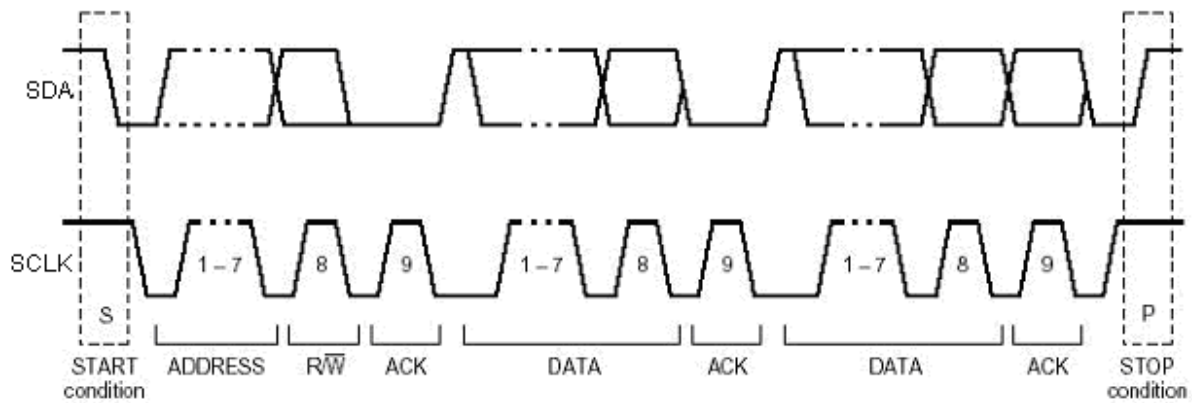
### 7.11.1. Addressing Setting

**Table 10. Addressing Setting**

| (MSB) | BIT |   |   |   |   |   | (LSB) |
|-------|-----|---|---|---|---|---|-------|
| 0     | 0   | 1 | 1 | 0 | 1 | 0 | RW    |

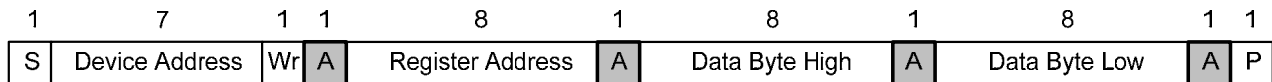
### 7.11.2. Complete Data Transfer

**Data Transfer over I<sup>2</sup>C Control Interface**



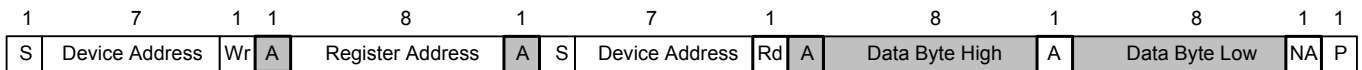
**Figure 15. Data Transfer Over I<sup>2</sup>C Control Interface**

### Write WORD Protocol



**Figure 16. Write WORD Protocol**

### Read WORD Protocol



|                                                                                                                                                                               |                                                                                                                         |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|
| <p>S: Start Condition</p> <p>Slave Address: 7-bit Device Address</p> <p>Wr: 0 for Write Command</p> <p>Rd: 1 for Read Command</p> <p>Command Code: 8-bit Register Address</p> | <p>A: 0 for ACK, 1 for NACK</p> <p>Data Byte: 16-bit Mixer data</p> <p>□: Master-to-Slave</p> <p>■: Slave-to-Master</p> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|

**Figure 17. Read WORD Protocol**

## 7.12. Odd-Addressed Register Access

The ALC5621 will return '0000h' when odd-addressed and unimplemented registers are read.

## 7.13. Power Management

The ALC5621 supports a grouped power down control register (Reg26). More detailed Power Management control is supported in Reg 3A, 3C, and 3E. Each particular block will only be active when both Reg26 and Reg3A/3C/3E are set to 'Enable'.

## 7.14. GPIO and Jack Detect Function

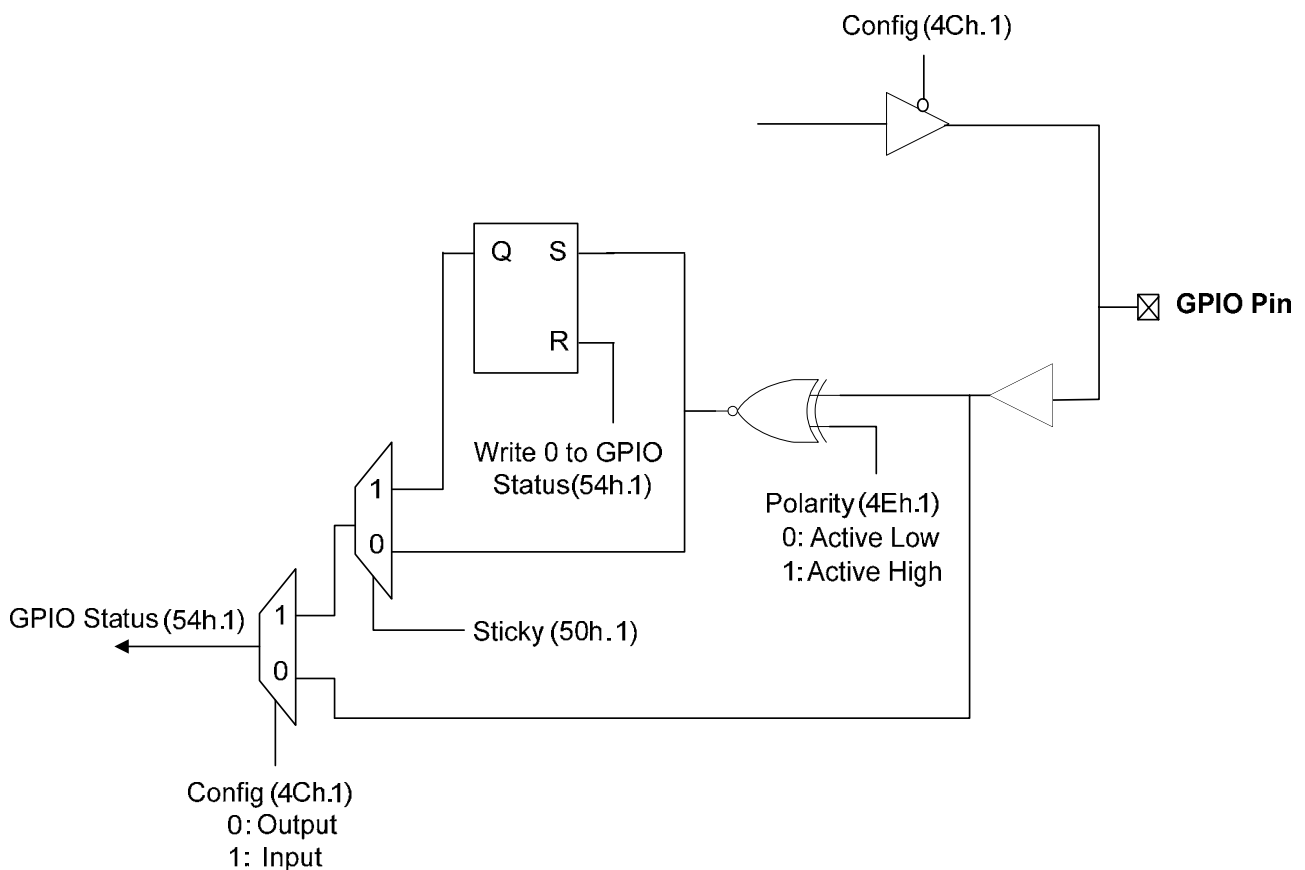
The GPIO pin of the ALC5621 can be configured to PLL\_OUT and IRQ\_Output by setting Reg-56[1:0]: gpio\_pin\_sharing.

The ALC5621 supports one GPIO that can be configured as Input/Output by Reg4C when gpio\_pin\_sharing = 00'b. When the GPIO is configured as Input, the status will be indicated in Reg54[1]. When the GPIO is configured as Output, Reg5C[1] is used to drive GPIO to High (1b) or Low (0b). The status can be read in Reg54[1].

In addition, the ALC5621 supports Jack Detect (JD1/JD2) to switch ON/OFF the Analog Output (Headphone Out, Speaker Out, and AUXOUT\_L/R).

JD1 and JD2 can be pin-shared from LINE\_IN\_R/L and are used to enable specified Analog audio output configured in the Reg-5Ah Jack Detect Control Register.

GPIO & JD input can be configured as sticky by setting Reg50, change polarity by setting Reg4E, and wake-up by setting Reg52 in order to generate the interrupt (IRQ). The driver can write each bit of Reg54 to '1' to clear each IRQ status flag.



**Figure 18. GPIO Implementation**



## 8. Mixer Registers List

Accessing odd numbered registers, or reading unimplemented registers, will return a 0.

### 8.1. *Reg-00h: Reset*

Default: 59B4h

**Table 11. Reg-00h: Reset**

| Name           | Bits  | Read/Write | Reset State | Description                              |
|----------------|-------|------------|-------------|------------------------------------------|
| Reserved       | 15    | R          | 0'h         | Reserved. Read as 0                      |
| REG-00_b14_b10 | 14:10 | R          | 16'h        | SE[4:0]=10110b                           |
| REG-00_b9      | 9     | R          | 0'h         | No Support for 20-Bit ADC                |
| REG-00_b8      | 8     | R          | 1'h         | Supports 16-Bit ADC                      |
| REG-00_b7      | 7     | R          | 1'h         | Supports 16-Bit DAC                      |
| REG-00_b6      | 6     | R          | 0'h         | No Support for 18-Bit DAC                |
| REG-00_b5      | 5     | R          | 1'h         | Support for Loudness                     |
| REG-00_b4      | 4     | R          | 1'h         | Headphone Output Support                 |
| Reserved       | 3     | R          | 0'h         | Reserved                                 |
| REG-00_b2      | 2     | R          | 1'h         | Supports EQ Control                      |
| Reserved       | 1     | R          | 0'h         | Reserved. Read as 0                      |
| REG-00_b0      | 0     | R          | 0'h         | Dedicated MIC PCM Input is Not Supported |

*Note: Writes to this register will reset all registers to their default values except PLL related registers. The written data will be ignored*

### 8.2. *Reg-02h: Speaker Output Volume*

Default: 8080h

**Table 12. Reg-02h: Speaker Output Volume**

| Name              | Bits | Read/Write | Reset State | Description                                                     |
|-------------------|------|------------|-------------|-----------------------------------------------------------------|
| sp_l_mute         | 15   | RW         | 1'h         | Mute SPK Left Control<br>0: On<br>1: Mute (-∞ dB)               |
| sp_l_dezero       | 14   | RW         | 0'h         | SPK Left Zero Cross Detector Control<br>0: Disable<br>1: Enable |
| sp_l_soft-mute_en | 13   | RW         | 0'h         | SPK Left_Softmute Enable<br>0: Disable<br>1: Enable             |
| sp_l_vol          | 12:8 | RW         | 0'h         | SPK Left Output Volume (SPKL[4:0]) in 1.5dB steps               |

| Name              | Bits | Read/Write | Reset State | Description                                                                                                                        |
|-------------------|------|------------|-------------|------------------------------------------------------------------------------------------------------------------------------------|
| sp_r_mute         | 7    | RW         | 1'h         | Mute SPK Right Control<br>0: On<br>1: Mute (-∞ dB)<br><i>Note: Not used when in differential mode (Reg1C[11:10])</i>               |
| sp_r_dezero       | 6    | RW         | 0'h         | SPK Right Zero Cross Detector Control<br>0: Disable<br>1: Enable<br><i>Note: Not used when in differential mode (Reg1C[11:10])</i> |
| sp_r_soft-mute_en | 5    | RW         | 0'h         | SPK Right_Softmute Enable<br>0: Disable<br>1: Enable<br><i>Note: Not used when in differential mode (Reg1C[11:10])</i>             |
| sp_r_vol          | 4:0  | RW         | 0'h         | SPK Right Output Volume (SPKR[4:0]) in 1.5dB Steps<br><i>Note: Not used when in differential mode (Reg1C[11:10])</i>               |

*Note: For SPKR/SPKL, 00h: 0dB attenuation*

*1Fh: 46.5dB attenuation*

### 8.3. Reg-04h: Headphone Output Volume

Default: 8080h

**Table 13. Reg-04h: Headphone Output Volume**

| Name              | Bits | Read/Write | Reset State | Description                                                                       |
|-------------------|------|------------|-------------|-----------------------------------------------------------------------------------|
| hp_l_mute         | 15   | RW         | 1'h         | Mute HP Left Control<br>0: On                      1: Mute Left Channel (-∞ dB)   |
| hp_l_dezero       | 14   | RW         | 0'h         | HP Left Zero Cross Detector Control<br>0: Disable              1: Enable          |
| hp_l_soft-mute_en | 13   | RW         | 0'h         | HP Left Channel Softmute Enable<br>0: Disable              1: Enable              |
| hp_l_vol          | 12:8 | RW         | 0'h         | Headphone Output Left Volume (HPL[4:0]) in 1.5dB Steps                            |
| hp_r_mute         | 7    | RW         | 1'h         | Mute HP Right Control<br>0: On                      1: Mute Right Channel (-∞ dB) |
| hp_r_dezero       | 6    | RW         | 0'h         | HP Right Zero Cross Detector Control<br>0: Disable              1: Enable         |
| hp_r_soft-mute_en | 5    | RW         | 0'h         | HP Right Channel Softmute Enable<br>0: Disable              1: Enable             |
| hp_r_vol          | 4:0  | RW         | 0'h         | Headphone Output Right Volume (HPR[4:0]) in 1.5dB Steps                           |

*Note: For HPR/HPL, 00h: 0dB attenuation*

*1Fh: 46.5dB attenuation*

## 8.4. Reg-06h: MONO\_OUT/AUXOUT Volume

Default: 8080h

**Table 14. Reg-06h: MONO\_OUT/AUXOUT Volume**

| Name                | Bits | Read/Write | Reset State | Description                                                                                                                       |
|---------------------|------|------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| AUXO_l_mute         | 15   | RW         | 1'h         | Mute Left Control<br>0: On                      1: Mute Left Channel (-∞ dB)                                                      |
| AUXO_l_dezero       | 14   | RW         | 0'h         | Left Zero Cross Detector Control<br>0: Disable              1: Enable                                                             |
| AUXO_l_soft-mute_en | 13   | RW         | 0'h         | AUXOUT Left Channel Softmute Enable<br>0: Disable              1: Enable                                                          |
| AUXO_l_vol          | 12:8 | RW         | 0'h         | AUXOUT Output Left Volume (AUXOLV[4:0]) In 1.5dB Steps                                                                            |
| AUXO_r_mute         | 7    | RW         | 1'h         | Mute Right Control<br>0: On                      1: Mute Right Channel (-∞ dB)<br><i>Note: Not used when in differential mode</i> |
| AUXO_r_dezero       | 6    | RW         | 0'h         | Right Zero Cross Detector Control<br>0: Disable              1: Enable<br><i>Note: Not used when in differential mode</i>         |
| AUXO_r_soft-mute_en | 5    | RW         | 0'h         | AUXOUT Right Channel Softmute Enable<br>0: Disable              1: Enable<br><i>Note: Not used when in differential mode</i>      |
| AUXO_r_vol          | 4:0  | RW         | 0'h         | AUXOUT Output Right Volume (AUXORV[4:0]) in 1.5dB Steps<br><i>Note: Not used when in differential mode</i>                        |

*Note: For AUXOL/R, 00h: 0dB attenuation*

*1Fh: 46.5dB attenuation*

## 8.5. Reg-08h: AUXIN Volume

Default: E808h

**Table 15. Reg-08h: AUXIN Volume**

| Name           | Bits | Read/Write | Reset State | Description                                                                               |
|----------------|------|------------|-------------|-------------------------------------------------------------------------------------------|
| auxi2hp_mute   | 15   | RW         | 1'h         | Mute AUXIN Volume Output to Headphone Mixer Control<br>0: On                      1: Mute |
| auxi2spk_mute  | 14   | RW         | 1'h         | Mute AUXIN Volume Output to Speaker Mixer Control<br>0: On                      1: Mute   |
| auxi2mono_mute | 13   | RW         | 1'h         | Mute AUXIN Volume Output to Mono Mixer Control<br>0: On                      1: Mute      |
| auxi_l_vol     | 12:8 | RW         | 08'h        | AUXIN Left Volume (AUXI LV [4:0]) in 1.5dB Steps                                          |
| Reserved       | 7:5  | R          | 0'h         | Reserved                                                                                  |
| auxi_r_vol     | 4:0  | RW         | 8'h         | AUXIN Right Volume (AUXIRV [4:0]) in 1.5dB Steps                                          |

*Note: For AUXIRV/AUXI LV, 00h: +12dB gain*

*08h: 0dB attenuation*

*1Fh: 34.5dB attenuation*

## 8.6. *Reg-0Ah: LINE\_IN Volume*

Default: E808h

**Table 16. Reg-0Ah: LINE\_IN Volume**

| Name         | Bits | Read/Write | Reset State | Description                                                                                 |
|--------------|------|------------|-------------|---------------------------------------------------------------------------------------------|
| li2hp_mute   | 15   | RW         | 1'h         | Mute LINE_IN Volume Output to Headphone Mixer Control<br>0: On                      1: Mute |
| li2spk_mute  | 14   | RW         | 1'h         | Mute LINE_IN Volume Output to Speaker Mixer Control<br>0: On                      1: Mute   |
| li2MONO_mute | 13   | RW         | 1'h         | Mute LINE_IN Volume Output to MONO Mixer Control<br>0: On                      1: Mute      |
| li_l_vol     | 12:8 | RW         | 08'h        | LINE_IN Left Volume (NLV[4:0]) in 1.5dB Steps                                               |
| Reserved     | 7:5  | R          | 0'h         | Reserved                                                                                    |
| li_r_vol     | 4:0  | RW         | 8'h         | LINE_IN Right Volume (NRV[4:0]) in 1.5dB Steps                                              |

*Note: For NRV/NLV, 00h: +12dB gain*

*08h: 0dB attenuation*

*1Fh: 34.5dB attenuation*

## 8.7. *Reg-0Ch: STEREO DAC Volume*

Default: E808h

**Table 17. Reg-0Ch: STEREO DAC Volume**

| Name          | Bits | Read/Write | Reset State | Description                                                                                    |
|---------------|------|------------|-------------|------------------------------------------------------------------------------------------------|
| dac2hp_mute   | 15   | RW         | 1'h         | Mute DAC Volume Output to Headphone Mixer Control<br>0: On                      1: Mute (-∞dB) |
| dac2spk_mute  | 14   | RW         | 1'h         | Mute DAC Volume Output to Speaker Mixer Control<br>0: On                      1: Mute (-∞dB)   |
| dac2MONO_mute | 13   | RW         | 1'h         | Mute DAC Volume Output to MONO Mixer Control<br>0: On                      1: Mute (-∞dB)      |
| dac_l_vol     | 12:8 | RW         | 08'h        | PCM Left DAC Volume (PLV[4:0]) in 1.5dB Steps                                                  |
| Reserved      | 7:5  | R          | 0'h         | Reserved                                                                                       |
| dac_r_vol     | 4:0  | RW         | 8'h         | PCM Right DAC Volume (PRV[4:0]) in 1.5dB Steps                                                 |

*Note: For PRV/PLV, 00h: +12dB gain*

*08h: 0dB attenuation*

*1Fh: 34.5dB attenuation*

## 8.8. *Reg-0Eh: MIC Volume*

Default: 0808h

**Table 18. Reg-0Eh: MIC Volume**

| Name     | Bits  | Read/Write | Reset State | Description                           |
|----------|-------|------------|-------------|---------------------------------------|
| Reserved | 15:13 | R          | 0'h         | Reserved                              |
| mic1_vol | 12:8  | RW         | 08'h        | MIC1 Volume (M1V[4:0]) in 1.5dB Steps |
| Reserved | 7:5   | R          | 0'h         | Reserved                              |
| mic2_vol | 4:0   | RW         | 8'h         | MIC2 Volume (M2V[4:0]) in 1.5dB Steps |

For M2V/M1V, 00h: +12dB gain

08h: 0dB attenuation

1Fh: 34.5dB attenuation

## 8.9. *Reg-10h: MIC Routing Control*

Default: E0E0h

**Table 19. Reg-10h: MIC Routing Control**

| Name           | Bits | Read/Write | Reset State | Description                                                                      |
|----------------|------|------------|-------------|----------------------------------------------------------------------------------|
| mic12hp_mute   | 15   | RW         | 1'h         | Mute MIC1 Volume Output to Headphone Mixer<br>0: On                      1: Mute |
| mic12spk_mute  | 14   | RW         | 1'h         | Mute MIC1 Volume Output to Speaker Mixer<br>0: On                      1: Mute   |
| mic12MONO_mute | 13   | RW         | 1'h         | Mute MIC1 Volume Output to MONO Mixer<br>0: On                      1: Mute      |
| mic1_diff_ctrl | 12   | RW         | 0'h         | MIC1 Differential Input Control<br>0: Disable              1: Enable             |
| Reserved       | 11:8 | R          | 0'h         | Reserved                                                                         |
| mic22hp_mute   | 7    | RW         | 1'h         | Mute MIC2 Volume Output to Headphone Mixer<br>0: On                      1: Mute |
| mic22spk_mute  | 6    | RW         | 1'h         | Mute MIC2 Volume Output to Speaker Mixer<br>0: On                      1: Mute   |
| mic22MONO_mute | 5    | RW         | 1'h         | Mute MIC2 Volume Output to MONO Mixer<br>0: On                      1: Mute      |
| mic2_diff_ctrl | 4    | RW         | 0'h         | MIC2 Differential Input Control<br>0: Disable              1: Enable             |
| Reserved       | 3:0  | R          | 0'h         | Reserved                                                                         |

## 8.10. Reg-12h: ADC Record Gain

Default: F58Bh

**Table 20. Reg-12h: ADC Record Gain**

| Name            | Bits | Read/Write | Reset State | Description                                                                                                         |
|-----------------|------|------------|-------------|---------------------------------------------------------------------------------------------------------------------|
| adc2hp_l_mute   | 15   | RW         | 1'h         | Mute Left Gain Output to Headphone Mixer Control<br>0: On 1: Mute ( $-\infty$ dB)                                   |
| adc2hp_r_mute   | 14   | RW         | 1'h         | Mute Right Gain Output to Headphone Mixer Control<br>0: On 1: Mute ( $-\infty$ dB)                                  |
| adc2MONO_l_mute | 13   | RW         | 1'h         | Mute Left Gain Output to MONO Mixer Control<br>0: On 1: Mute ( $-\infty$ dB)                                        |
| adc2MONO_r_mute | 12   | RW         | 1'h         | Mute Right Gain Output to MONO Mixer Control<br>0: On 1: Mute ( $-\infty$ dB)                                       |
| adc_l_vol       | 11:7 | RW         | 0B'h        | ADC Record Gain Left Channel (LRG[4:0]) in 1.5dB Steps<br>00h: -16.5dB attenuation 0Bh: 0dB gain<br>1Fh: 30dB gain  |
| adc_l_dezero    | 6    | RW         | 0'h         | ADC_L Zero-Cross Detector Control<br>0: Disable 1: Enable                                                           |
| adc_r_dezero    | 5    | RW         | 0'h         | ADC_R Zero-Cross Detector Control<br>0: Disable 1: Enable                                                           |
| adc_r_vol       | 4:0  | RW         | 0B'h        | ADC Record Gain Right Channel (RRG[4:0]) in 1.5dB Steps<br>00h: -16.5dB attenuation 0Bh: 0dB gain<br>1Fh: 30dB gain |

## 8.11. Reg-14h: ADC Record Mixer Control

Default: 7F7Fh

**Table 21. Reg-14h: ADC Record Mixer Control**

| Name          | Bits | Read/Write | Reset State | Description                                                                                                                                                                                                     |
|---------------|------|------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved      | 15   | R          | 0'h         | Reserved                                                                                                                                                                                                        |
| adcrec_l_mute | 14:8 | RW         | 7F'h        | Left Mixer Mute Control<br>0: On 1: Mute ( $-\infty$ dB)<br>Bit 14: MIC1 Bit 13: MIC2<br>Bit 12: LINE_IN_L Bit 11: AUXIN_L<br>Bit 10: Headphone Mixer Left Channel<br>Bit 9: Speaker Mixer<br>Bit 8: MONO Mixer |
| Reserved      | 7    | R          | 0'h         | Reserved                                                                                                                                                                                                        |
| adcrec_r_mute | 6:0  | RW         | 7F'h        | Right Mixer Mute Control<br>0: On 1: Mute ( $-\infty$ dB)<br>Bit 6: MIC1 Bit 5: MIC2<br>Bit 4: LINE_IN_R Bit 3: AUXIN_R<br>Bit 2: Headphone Mixer Right Channel<br>Bit 1: Speaker Mixer<br>Bit 0: MONO Mixer    |

## 8.12. Reg-16h: Avol Soft Volume Control Time

Default: 0000h

**Table 22. Reg-16h: Avol Soft Volume Control Time**

| Name                  | Bits | Read/Write | Reset State | Description                                                                                                                                                                                                                                                                         |
|-----------------------|------|------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved              | 15:4 | R          | 000'h       | Reserved                                                                                                                                                                                                                                                                            |
| soft_volume_ctrl_avol | 3:0  | RW         | 1010'b      | Soft Volume Control Time (Default=1001b)<br>0000: 1 SVSYNC      0001: 2 SVSYNC<br>0010: 4 SVSYNC      0011: 8 SVSYNC<br>0100: 16 SVSYNC     0101: 32 SVSYNC<br>0110: 64 SVSYNC     0111: 128 SVSYNC<br>1000: 256 SVSYNC    1001: 512 SVSYNC<br>1010: 1024 SVSYNC   Others: Reserved |

Note: SVSYNC=1/Fs, Step:-1.5dBFS

## 8.13. Reg-1Ch: Output Mixer Control

Default: C000h

**Table 23. Reg-1Ch: Output Mixer Control**

| Name             | Bits  | Read/Write | Reset State | Description                           |                     |                             |
|------------------|-------|------------|-------------|---------------------------------------|---------------------|-----------------------------|
| spk_outn_souce   | 15:14 | RW         | 3'h         | SPK_Out_N Source Select               |                     |                             |
|                  |       |            |             |                                       | spk_vol_in_sel='01' | spk_vol_in_sel='10' or '11' |
|                  |       |            |             | 00                                    | RN                  | -(L+R)                      |
|                  |       |            |             | 01                                    | RP                  | L+R                         |
|                  |       |            |             | 10                                    | LN                  | -(L+R)                      |
|                  |       |            |             | 11                                    | Vmid                |                             |
| spk_out_type_sel | 13    | RW         | 0'h         | SPK_Output Type Select<br>0: Class-AB |                     |                             |

## 8.14. Reg-22h: Microphone Control

Default: 0000h

**Table 24. Reg-22h: Microphone Control**

| Name                   | Bits  | Read/Write | Reset State | Description                                                                                                    |
|------------------------|-------|------------|-------------|----------------------------------------------------------------------------------------------------------------|
| Reserved               | 15:12 | R          | 0'h         | Reserved                                                                                                       |
| mic1_boost_ctrl        | 11:10 | RW         | 0'h         | MIC1 Boost Control<br>00: Bypass                      01: +20dB<br>10: +30dB                      11: Reserved |
| mic2_boost_ctrl        | 9:8   | RW         | 0'h         | MIC2 Boost Control<br>00: Bypass                      01: +20dB<br>10: +30dB                      11: Reserved |
| Reserved               | 7:6   | R          | 0'h         | Reserved. Read as 0                                                                                            |
| mic1_bias_voltage_ctrl | 5     | RW         | 0'h         | MICBIAS1 Output Voltage Control<br>0: 0.9*AVDD                      1: 0.75*AVDD                               |
| Reserved               | 4:2   | R          | 0'h         | Reserved. Read as 0                                                                                            |
| mic_bias_threshold     | 1:0   | RW         | 0'h         | MICBIAS1/2 Short Current Detector Threshold<br>00: 600μA                      01: 1200μA<br>1x: 1800μA         |

## 8.15. Reg-34h: Digital Audio Interface Control

Default: 8000h

**Table 25. Reg-34h: Audio Interface**

| Name                          | Bits | Read/Write | Reset State | Description                                                                                                                                                      |
|-------------------------------|------|------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| stereo_i2s_mode_sel           | 15   | RW         | 1'h         | Main Serial Data Port Mode Selection<br>0: Master                      1: Slave                                                                                  |
| pcm_mode_sel                  | 14   | RW         | 0'h         | PCM Mode Select<br>0: Mode A                      1: Mode B                                                                                                      |
| Reserved                      | 13:8 | RW         | 0'h         | Reserved                                                                                                                                                         |
| stereo_i2s_bclk_polarity_ctrl | 7    | RW         | 0'h         | Stereo I <sup>2</sup> S BCLK Polarity Control<br>0: Normal                      1: Invert                                                                        |
| Reserved                      | 6    | RW         | 0'h         | Reserved                                                                                                                                                         |
| adclckswap                    | 5    | RW         | 0'b         | ADC Data L/R Swap<br>0: ADC data appear at left phase of LRCK<br>1: ADC data appear at right phase of LRCK<br><i>Note: Supported in I<sup>2</sup>S &amp; PCM</i> |
| dacclckswap                   | 4    | RW         | 0'b         | DAC Data L/R Swap<br>0: DAC data appear at left phase of LRCK<br>1: DAC data appear at right phase of LRCK<br><i>Note: Supported in I<sup>2</sup>S &amp; PCM</i> |

| Name                       | Bits | Read/Write | Reset State | Description                                                                                                                                                        |
|----------------------------|------|------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| stereo_i2s_data_len_sel    | 3:2  | RW         | 0'h         | Data Length Selection<br>00: 16 bits                      01: 20 bits<br>10: 24 bits                      11: 32 bits                                              |
| stereo_i2s_data_format_sel | 1:0  | RW         | 0'h         | Stereo PCM Data Format Selection<br>00: I <sup>2</sup> S format                      01: Right justified<br>10: Left justified                      11: PCM format |

## 8.16. Reg-36Ah: Stereo AD/DA Clock Control

Default: 166Dh

**Table 26. Reg-36h: Stereo AD/DA Clock Control**

| Name             | Bits  | Read/Write | Reset State | Description                                                                                                                                                                                                          |
|------------------|-------|------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved         | 15    | RW         | 0'h         | Reserved                                                                                                                                                                                                             |
| i2s_pre_div      | 14:12 | RW         | 1'h         | I2S_Pre_Div<br>000b: ÷1                      001b: ÷2                      010b: ÷4<br>011b: ÷8                      100b: ÷16                      101b: ÷32<br>Others: Reserved                                    |
| i2s_selclk_div   | 11:9  | RW         | 011'b       | I2S_BCLK_Div<br>000b: ÷1 (MCLK=BCLK)                      001b: ÷2<br>010b: ÷3                      011b: ÷4                      100b: ÷6<br>101b: ÷8                      110b: ÷12                      111b: ÷16 |
| i2s_wclk_div_pre | 8:5   | RW         | 0011'b      | I2S_WCLK_Div_pre<br>0000b: ÷1                      0001b: ÷2                      0010b: ÷3<br>.....<br>1101b: ÷14                      1110b: ÷15                      1111b: ÷16                                   |
| i2s_wclk_div     | 4:2   | RW         | 011'b       | I2S_WCLK_Div<br>000b: ÷2                      001b: ÷4                      010b: ÷8<br>011b: ÷16                      100b: ÷32                      Others: Reserved                                               |
| adda_filter_clk  | 1     | RW         | 0'b         | Stereo ADDA Filter Clock Select<br>0b: 256Fs                      1b: 384Fs                                                                                                                                          |
| adda_osr         | 0     | RW         | 1'b         | Stereo ADDA Over Sample Rate Select<br>0b: Low                      1b: High                                                                                                                                         |

## 8.17. Reg-38h: Companding Control

Default: 0000h

**Table 27. Reg-38h: Companding Control**

| Name          | Bits | Read/Write | Reset State | Description                                                                                                                   |
|---------------|------|------------|-------------|-------------------------------------------------------------------------------------------------------------------------------|
| word_length_8 | 15   | RW         | 0'b         | 0: OFF<br>1: Device works in 8 bits mode when in PCM mode B                                                                   |
| Reserved      | 14:4 | RW         | 0'h         | Reserved                                                                                                                      |
| adc_comp      | 3:2  | RW         | 00'b        | ADC Companding (for ADC DAT Output)<br>00: OFF                      01: $\mu$ -Law<br>10: A-Law                  11: Reserved |
| dac_comp      | 1:0  | RW         | 00'b        | DAC Companding (for DAC DAT Input)<br>00: OFF                      01: $\mu$ -Law<br>10: A-Law                  11: Reserved  |

## 8.18. Reg-3Ah: Power Management Addition 1

Default: 0000h

**Table 28. Reg-3Ah: Power Management Addition 1**

| Name                   | Bits  | Read/Write | Reset State | Description                                                                                                                                                               |
|------------------------|-------|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Main_i2s_en            | 15    | RW         | 0'h         | I <sup>2</sup> S Digital Interface Enable<br>0: Disable                  1: Enable                                                                                        |
| pow_zcd                | 14    | RW         | 0'h         | All Zero Cross Detect Power Down<br>0: Disable                  1: Enable                                                                                                 |
| Reserved               | 13:12 | RW         | 0'h         | Reserved                                                                                                                                                                  |
| pow_mic1_bias          | 11    | RW         | 0'h         | 0: Disable                  1: Enable microphone1 bias                                                                                                                    |
| pow_mic1_bias_det_ctrl | 10    | RW         | 0'h         | MICBIAS1 Short Current Detector Control<br>0: Disable                  1: Enable                                                                                          |
| Reserved               | 9     | RW         | 0'h         | Reserved                                                                                                                                                                  |
| pow_softgen            | 8     | RW         | 0'h         | Power on Softgen<br>1: Power on              0: Power down<br><i>Note: Refer to the ALC5621 application note for detailed de-pop sequence information.</i>                |
| Reserved               | 7     | RW         | 0'h         | Reserved                                                                                                                                                                  |
| pow_dpbuf_hp           | 6     | RW         | 0'h         | Power on Headphone Depop Buffer<br>1: Power on              0: Power down<br><i>Note: Refer to the ALC5621 application note for detailed de-pop sequence information.</i> |
| en_hp_out_amp          | 5     | RW         | 0'h         | Headphone Output Amplifier Buffer<br>1: Enable HP Output buffer for normal loading >K $\Omega$<br>0: Disable (DPOP mode)                                                  |

| Name               | Bits | Read/Write | Reset State | Description                                                                                                                                               |
|--------------------|------|------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| en_hp_enhance_amp  | 4    | RW         | 0'h         | Headphone Enhance Output Buffer<br>1: Enable HP Output buffer for small R loading (<100Ω)<br>0: Disable (DPOP mode or normal loading mode)                |
| Reserved           | 3    | RW         | 0'h         | Reserved                                                                                                                                                  |
| pow_dpbuf_aux      | 2    | RW         | 0'h         | AUX Power on Depop Buffer<br>1: Power on<br>0: Power down<br><i>Note: Refer to the ALC5621 application note for detailed de-pop sequence information.</i> |
| en_aux_out_amp     | 1    | RW         | 0'h         | AUX Output Amplifier Buffer<br>1: Enable AUX Output buffer for normal loading (>KΩ)<br>0: Disable (DPOP mode)                                             |
| en_aux_enhance_amp | 0    | RW         | 0'h         | Enhanced AUX Amplifier Output Buffer<br>1: Enable AUX Output buffer for small R loading (<100Ω)<br>0: Disable (DPOP mode or normal loading mode)          |

### 8.18.1. Headphone Output Amplifier Configuration

**Table 29. Headphone Output Amplifier Configuration**

| en_hp_out_amp | en_hp_enhance_amp | Description                             |
|---------------|-------------------|-----------------------------------------|
| 0'b           | 0'b               | HP Output OFF                           |
| 0'b           | 1'b               | Not Used                                |
| 1'b           | 0'b               | HP Output for Normal Loading (>Kohm)    |
| 1'b           | 1'b               | HP Output for Small R Loading (<100ohm) |

### 8.18.2. Auxiliary Output Amplifier Configuration

**Table 30. Auxiliary Output Amplifier Configuration**

| en_aux_out_amp | en_aux_enhance_amp | Description                              |
|----------------|--------------------|------------------------------------------|
| 0'b            | 0'b                | AUX Output OFF                           |
| 0'b            | 1'b                | Not Used                                 |
| 1'b            | 0'b                | AUX output for Normal Loading (>Kohm)    |
| 1'b            | 1'b                | AUX output for small R Loading (<100ohm) |

## 8.19. Reg-3Ch: Power Management Addition 2

Default: 0000h

**Table 31. Reg-3Ch: Power Management Addition 2**

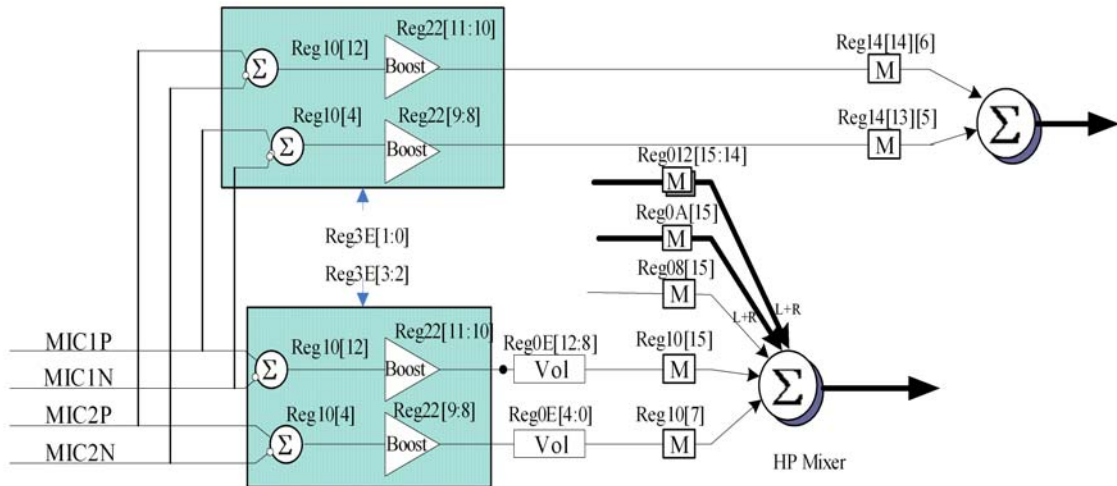
| Name              | Bits | Read/Write | Reset State | Description                                                                                                 |
|-------------------|------|------------|-------------|-------------------------------------------------------------------------------------------------------------|
| pow_clsab         | 15   | RW         | 0'h         | Class-AB Power (All)<br>0: Disable 1: Enable                                                                |
| pow_clsd          | 14   | RW         | 0'b         | Class-D Power (All)<br>0: Disable 1: Enable                                                                 |
| pow_vref          | 13   | RW         | 0'h         | VREF of All Analog Circuits<br>0: Disable 1: Enable<br><i>Note: This bit works only if Index-39[11]=0b.</i> |
| pow_pll           | 12   | RW         | 0'h         | PLL<br>0: Disable 1: Enable                                                                                 |
| Reserved          | 11   | RW         | 0'h         | Reserved.<br>Must be kept to 0.                                                                             |
| pow_dac_ref       | 10   | RW         | 0'h         | Power DAC Reference Circuit (Vref+/Vref-)<br>0: Disable 1: Enable                                           |
| pow_dac_l         | 9    | RW         | 0'h         | Left Stereo DAC Filter Clock<br>0: Disable 1: Enable                                                        |
| pow_dac_r         | 8    | RW         | 0'h         | Right Stereo DAC Filter Clock<br>0: Disable 1: Enable                                                       |
| pow_adc_l         | 7    | RW         | 0'h         | Left Stereo ADC Filter Clock and Input Gain<br>0: Disable 1: Enable                                         |
| pow_adc_r         | 6    | RW         | 0'h         | Right Stereo ADC Filter Clock and Input Gain<br>0: Disable 1: Enable                                        |
| pow_mix_hp_l      | 5    | RW         | 0'h         | Left Headphone Mixer<br>0: Disable 1: Enable                                                                |
| pow_mix_hp_r      | 4    | RW         | 0'h         | Right Headphone Mixer<br>0: Disable 1: Enable                                                               |
| pow_mix_spk       | 3    | RW         | 0'h         | Speaker Mixer<br>0: Disable 1: Enable                                                                       |
| pow_mix_mono      | 2    | RW         | 0'h         | MONO Mixer<br>0: Disable 1: Enable                                                                          |
| pow_mix_adc_rec_l | 1    | RW         | 0'h         | Left ADC Record Mixer<br>0: Disable 1: Enable                                                               |
| pow_mix_adc_rec_r | 0    | RW         | 0'h         | Right ADC Record Mixer<br>0: Disable 1: Enable                                                              |

## 8.20. Reg-3Eh: Power Management Addition 3

Default: 0000h

**Table 32. Reg-3Eh: Power Management Addition 3**

| Name             | Bits | Read/Write | Reset State | Description                                                                                                                               |
|------------------|------|------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| pow_main_bias    | 15   | RW         | 0'h         | Main Bias Analog Circuit<br>0: Disable                      1: Enable                                                                     |
| pow_aux_outl_vol | 14   | RW         | 0'h         | AUXOUT_L(Mono_P) Volume Control & AUX_L Amplifier<br>0: Disable                      1: Enable                                            |
| pow_aux_outr_vol | 13   | RW         | 0'h         | AUXOUT_R(Mono_N) Volume Control & AUX_R Amplifier<br>0: Disable                      1: Enable                                            |
| pow_spk          | 12   | RW         | 0'h         | SPK_OUT Output<br>0: Disable                      1: Enable<br><i>Note: pow_spk controls the speaker output of Class-AB &amp; Class-D</i> |
| Reserved         | 11   | RW         | 0'h         | Reserved                                                                                                                                  |
| pow_hp_l_vol     | 10   | RW         | 0'h         | HP_OUT_L Volume Control (Amp)<br>0: Disable                      1: Enable                                                                |
| pow_hp_r_vol     | 9    | RW         | 0'h         | HP_OUT_R Volume Control (Amp)<br>0: Disable                      1: Enable                                                                |
| Reserved         | 8    | RW         | 0'h         | Reserved                                                                                                                                  |
| pow_li_l_vol     | 7    | RW         | 0'h         | LINE_IN Left Volume Control<br>0: Disable                      1: Enable                                                                  |
| pow_li_r_vol     | 6    | RW         | 0'h         | LINE_IN Right Volume Control<br>0: Disable                      1: Enable                                                                 |
| pow_auxin_l_vol  | 5    | RW         | 0'h         | AUXIN Left Volume Control<br>0: Disable                      1: Enable                                                                    |
| pow_auxin_r_vol  | 4    | RW         | 0'h         | AUXIN Right Volume Control<br>0: Disable                      1: Enable                                                                   |
| pow_mic1_vol     | 3    | RW         | 0'h         | MIC1 Boost + Differential Mixer + Volume Amp Control<br>0: Disable                      1: Enable                                         |
| pow_mic2_vol     | 2    | RW         | 0'h         | MIC2 Boost+ Differential Mixer + Volume Amp Control<br>0: Disable                      1: Enable                                          |
| pow_mic1_admixer | 1    | RW         | 0'h         | MIC1 AD Boost + AD Differential Mixer<br>0: Disable                      1: Enable                                                        |
| pow_mic2_admixer | 0    | RW         | 0'h         | MIC2 AD Boost + AD Differential Mixer<br>0: Disable                      1: Enable                                                        |



**Figure 20. Power Control to MIC Input**

## 8.21. Reg-40h: Additional Control Register

Default: 5300h

**Table 33. Reg-40h: Additional Control Register**

| Name              | Bits  | Read/Write | Reset State | Description                                                                                                                                                                                             |
|-------------------|-------|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| se_diff_auxout    | 15    | RW         | 0'b         | AUXOUT Selection of Single-Ended or Differential Mode<br>0: Differential Mode      1: Single-Ended Mode                                                                                                 |
| spk_ampAB_ctrl    | 14:12 | RW         | 5'h         | Speaker Class-AB Amplifier $V_{MID}$ Ratio Control (Output Gain Control)<br>000: 2.25 Vdd      001: 2.00 Vdd<br>010: 1.75 Vdd      011: 1.5 Vdd<br>100: 1.25 Vdd      101: 1 Vdd<br>Others: Not allowed |
| spk_ampD_ctrl     | 11:10 | RW         | 0'h         | Speaker Class-D Amplifier $V_{MID}$ Ratio Control (Output Gain Control)<br>00: 1.75 Vdd      01: 1.5 Vdd<br>10: 1.25 Vdd      11: 1.0 Vdd                                                               |
| dac_hpf_en        | 9     | RW         | 1'h         | STEREO DAC High Pass Filter<br>0: Disable      1: Enable                                                                                                                                                |
| adc_hpf_en        | 8     | RW         | 1'h         | STEREO ADC High Pass Filter<br>0: Disable      1: Enable                                                                                                                                                |
| Reserved          | 7:6   | R          | 0'h         | Reserved                                                                                                                                                                                                |
| digital_vol_boost | 5:4   | RW         | 0'b         | Digital Volume Boost<br>00: 0dB      01: 6dB<br>10: 12dB      11: 18dB                                                                                                                                  |
| se_btl_clsab      | 3     | RW         | 0'b         | Speaker Class-AB Selection of Single-Ended or Bridge-Tied Load (BTL)<br>0: Differential Mode      1: Single-Ended Mode                                                                                  |
| Reserved          | 2:0   | RW         | 0'h         | Reserved                                                                                                                                                                                                |

## 8.22. Reg-42h: Global Clock Control Register

Default: 0000h

**Table 34. Reg-42h: Global Clock Control Register**

| Name             | Bits | Read/Write | Reset State | Description                                                                                                                              |
|------------------|------|------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------|
| sel_sysclk       | 15   | RW         | 0'h         | Clock Source MUX Control<br>0: MCLK                      1: PLL Output                                                                   |
| pll_sour_sel     | 14   | RW         | 0'h         | PLL Source Select<br>0: From MCLK              1: From BLCK                                                                              |
| Reserved         | 13:3 | RW         | 0'h         | Reserved                                                                                                                                 |
| pllout_div_ratio | 2:1  | RW         | 0'b         | PLL Output Division Ratio<br>(Divider of PLL Output to GPIO)<br>00: ÷1                      01: ÷2<br>10: ÷4                      11: ÷8 |
| pll_pre_div      | 0    | RW         | 0'b         | PLL Pre-Divider<br>0b: ÷1                      1b: ÷2                                                                                    |

## 8.23. Reg-44h: PLL Control Register

### 8.23.1. Reg-44h: PLL Control Register

Default: 0000h

**Table 35. Reg-44h: PLL Control Register**

| Name         | Bits | Read/Write | Reset State | Description                                                                                    |
|--------------|------|------------|-------------|------------------------------------------------------------------------------------------------|
| pll_n_code   | 15:8 | RW         | 00'h        | N[7:0] Code for Analog PLL<br>00000000: Div 2<br>00000001: Div 3<br>.....<br>11111111: Div 257 |
| pll_m_bypass | 7    | RW         | 0'h         | Bypass PLL M<br>0b: No bypass<br>1b: Bypass                                                    |
| pll_k_code   | 6:4  | RW         | 0'h         | K[2:0] Code for Analog PLL<br>000: Div 2<br>001: Div 3<br>.....<br>111: Div 9                  |
| pll_m_code   | 3:0  | RW         | 0'h         | M[3:0] Code for Analog PLL<br>0000: Div 2<br>0001: Div 3<br>.....<br>1111: Div 17              |

Note: The PLL1 transmit formula is  $F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2))$  {Typical K=2}

### 8.23.2. PLL Clock Setting Table for 48K: (Unit: MHz)

**Table 36. PLL Clock Setting Table for 48K: (Unit: MHz)**

| MCLK   | N  | M  | F <sub>VCO</sub> | K | F <sub>OUT</sub> |
|--------|----|----|------------------|---|------------------|
| 13     | 66 | 7  | 98.222           | 2 | 24.555           |
| 3.6864 | 78 | 1  | 98.304           | 2 | 24.576           |
| 2.048  | 94 | 0  | 98.304           | 2 | 24.576           |
| 4.096  | 70 | 1  | 98.304           | 2 | 24.576           |
| 12     | 80 | 8  | 98.4             | 2 | 24.6             |
| 15.36  | 81 | 11 | 98.068           | 2 | 24.517           |
| 16     | 78 | 11 | 98.462           | 2 | 24.615           |
| 19.2   | 80 | 14 | 98.4             | 2 | 24.6             |
| 19.68  | 78 | 14 | 98.4             | 2 | 24.6             |

### 8.23.3. PLL Clock Setting Table for 44.1K: (Unit: MHz)

**Table 37. PLL Clock Setting Table for 44.1K: (Unit: MHz)**

| MCLK   | N  | M  | F <sub>VCO</sub> | K | F <sub>OUT</sub> |
|--------|----|----|------------------|---|------------------|
| 13     | 68 | 8  | 91               | 2 | 22.75            |
| 3.6864 | 72 | 1  | 90.931           | 2 | 22.733           |
| 2.048  | 86 | 0  | 90.112           | 2 | 22.528           |
| 4.096  | 64 | 1  | 90.112           | 2 | 22.528           |
| 12     | 66 | 7  | 90.667           | 2 | 22.667           |
| 15.36  | 63 | 9  | 90.764           | 2 | 22.691           |
| 16     | 66 | 10 | 90.667           | 2 | 22.667           |
| 19.2   | 64 | 12 | 90.514           | 2 | 22.629           |
| 19.68  | 67 | 13 | 90.528           | 2 | 22.632           |

## 8.24. Reg-4Ah: GPIO\_Output Pin Control

Default: 0000h

**Table 38. Reg-4Ch: GPIO\_Output Pin Control**

| Name            | Bits | Read/Write | Reset State | Description                                                |
|-----------------|------|------------|-------------|------------------------------------------------------------|
| Reserved        | 15:2 | R          | 0000'h      | Reserved                                                   |
| gpio_out_status | 1    | RW         | 0'h         | GPIO Output Pin Control<br>0b: Drive Low<br>1b: Drive High |
| Reserved        | 0    | R          | 0'h         | Reserved. Read as 0                                        |

## 8.25. Reg-4Ch: GPIO Pin Configuration

Default: 1C0Eh

**Table 39. Reg-4Ch: GPIO Pin Configuration**

| Name                | Bits  | Read/Write | Reset State | Description                                                                                   |
|---------------------|-------|------------|-------------|-----------------------------------------------------------------------------------------------|
| Reserved            | 15:13 | R          | 00'h        | Reserved                                                                                      |
| over_curr_spk_conf  | 12    | RW         | 1'h         | Speaker Over-Current Status Source Configuration<br>0: Bypass                      1: Normal  |
| Reserved            | 11    | RW         | 1'h         | Reserved                                                                                      |
| mic1_short_det_conf | 10    | RW         | 1'h         | MICBIAS Short Current Status Source Configuration<br>0: Bypass                      1: Normal |
| Reserved            | 9:4   | R          | 0'h         | Reserved                                                                                      |
| jd2_conf            | 3     | RW         | 1'h         | Jack Detect 2 Status Source Configuration<br>0: Bypass                      1: Normal         |
| jd1_conf            | 2     | RW         | 1'h         | Jack Detect 2 Status Source Configuration<br>0: Bypass                      1: Normal         |
| gpio_conf           | 1     | RW         | 1'h         | GPIO Pin Configuration<br>0: Bypass                      1: Input                             |
| Reserved            | 0     | R          | 0'h         | Reserved. Read as 0                                                                           |

## 8.26. Reg-4Eh: GPIO Pin Polarity

Default: 1C0Eh

**Table 40. Reg-4Eh: GPIO Pin Polarity**

| Name                    | Bits  | Read/Write | Reset State | Description                                                                                |
|-------------------------|-------|------------|-------------|--------------------------------------------------------------------------------------------|
| Reserved                | 15:13 | R          | 00'h        | Reserved                                                                                   |
| over_curr_spk_polarity  | 12    | RW         | 1'h         | Speaker Over-Current Polarity<br>0: Low Active                      1: High Active         |
| Reserved                | 11    | RW         | 1'h         | Reserved                                                                                   |
| mic1_short_det_polarity | 10    | RW         | 1'h         | MICBIAS Short Current Detect Polarity<br>0: Low Active                      1: High Active |
| Reserved                | 9:4   | R          | 0'h         | Reserved                                                                                   |
| jd2_polarity            | 3     | RW         | 1'h         | Jack Detect 2 Pin Polarity<br>0: Low Active                      1: High Active            |
| jd1_polarity            | 2     | RW         | 1'h         | Jack Detect 1 Pin Polarity<br>0: Low Active                      1: High Active            |
| gpio_polarity           | 1     | RW         | 1'h         | GPIO Pin Polarity<br>0: Low Active                      1: High Active                     |
| Reserved                | 0     | R          | 0'h         | Reserved. Read as 0                                                                        |

## 8.27. Reg-50h: GPIO Pin Sticky

Default: 0000h

**Table 41. Reg-50h: GPIO Pin Sticky**

| Name                     | Bits  | Read/Write | Reset State | Description                                                                                |
|--------------------------|-------|------------|-------------|--------------------------------------------------------------------------------------------|
| Reserved                 | 15:13 | R          | 00'b        | Reserved                                                                                   |
| over_curr_spk_sticky_en  | 12    | RW         | 0'h         | Speaker Over-Current Sticky Enable<br>0: Not sticky                      1: Sticky         |
| Reserved                 | 11    | RW         | 0'h         | Reserved                                                                                   |
| mic1_short_det_sticky_en | 10    | RW         | 0'h         | MICBIAS Short Current Detect Sticky Enable<br>0: Not sticky                      1: Sticky |
| Reserved                 | 9:4   | R          | 0'h         | Reserved                                                                                   |
| jd2_sticky_En            | 3     | RW         | 0'h         | Jack Detect 2 Pin Sticky Enable<br>0: Not sticky                      1: Sticky            |
| jd1_sticky_En            | 2     | RW         | 0'h         | Jack Detect 1 Pin Sticky Enable<br>0: Not sticky                      1: Sticky            |
| gpio_sticky_En           | 1     | RW         | 0'h         | GPIO Pin Sticky Enable<br>0: Not sticky                      1: Sticky                     |
| Reserved                 | 0     | R          | 0'h         | Reserved. Read as 0                                                                        |

## 8.28. Reg-52h: GPIO Pin Wake-Up

Default: 0000h

**Table 42. Reg-52h: GPIO Pin Wake-Up**

| Name                     | Bits  | Read/Write | Reset State | Description                                                                                  |
|--------------------------|-------|------------|-------------|----------------------------------------------------------------------------------------------|
| Reserved                 | 15:13 | R          | 00'b        | Reserved                                                                                     |
| over_curr_spk_wakeup_en  | 12    | RW         | 0'h         | Speaker Over-Current Wake-Up Enable<br>0: No wake-up                      1: Wake up         |
| Reserved                 | 11    | RW         | 0'h         | Reserved                                                                                     |
| mic1_short_det_wakeup_en | 10    | RW         | 0'h         | MICBIAS Short Current Detect Wake-Up Enable<br>0: No wake-up                      1: Wake up |
| Reserved                 | 9:4   | R          | 0'h         | Reserved                                                                                     |
| jd2_wakeup_en            | 3     | RW         | 0'h         | Jack Detect 2 Pin Wake-Up Enable<br>0: No wake-up                      1: Wake up            |
| jd1_wakeup_en            | 2     | RW         | 0'h         | Jack Detect 1 Pin Wake-Up Enable<br>0: No wake-up                      1: Wake up            |
| gpio_wakeup_en           | 1     | RW         | 0'h         | GPIO Pin Wake-Up Enable<br>0: No wake-up                      1: Wake up                     |
| Reserved                 | 0     | R          | 0'h         | Reserved. Read as 0                                                                          |

## 8.29. Reg-54h: GPIO Pin Status

Default: 0002h

**Table 43. Reg-54h: GPIO Pin Status**

| Name                  | Bits  | Read/Write | Reset State | Description                                                                                            |
|-----------------------|-------|------------|-------------|--------------------------------------------------------------------------------------------------------|
| Reserved              | 15:13 | R          | 00'b        | Reserved                                                                                               |
| over_curr_spk_status  | 12    | R          | 0'h         | Speaker Over-Current Status<br>Read: Return status<br>Write: Writing '0' clears sticky bit             |
| Reserved              | 11    | R          | 0'h         | Reserved                                                                                               |
| mic1_short_det_status | 10    | R          | 0'h         | MICBIAS Short Current Detect Status<br>Read: Return status<br>Write: Writing '0' clears the sticky bit |
| Reserved              | 9:4   | R          | 0'h         | Reserved                                                                                               |
| jd2_status            | 3     | R          | 0'h         | Jack Detect 2 Pin Status<br>Read: Returns status of JD2 pin<br>Write: Writing '0' clears sticky bit    |
| jd1_status            | 2     | R          | 0'h         | Jack Detect 1 Pin Status<br>Read: Return status of JD1 pin<br>Write: Writing '0' clears sticky bit     |
| gpio_status           | 1     | R          | 1'h         | GPIO Pin Status<br>Read: Returns status of each GPIO pin<br>Write: Writing '0' clears the sticky bit   |
| Reserved              | 0     | R          | 0'h         | Reserved. Read as 0                                                                                    |

## 8.30. Reg-56h: Pin Sharing

Default: 0000h

**Table 44. Reg-56h: Pin Sharing**

| Name                | Bits | Read/Write | Reset State | Description                                                                    |
|---------------------|------|------------|-------------|--------------------------------------------------------------------------------|
| lineinl_pin_sharing | 15   | RW         | 0'b         | LINE_IN_L Pin Sharing<br>0: LINE_IN_L      1: JD1                              |
| lineinr_pin_sharing | 14   | RW         | 0'h         | LINE_IN_R Pin Sharing<br>0: LINE_IN_R      1: JD2                              |
| Reserved            | 13:2 | RW         | 000'h       | Reserved                                                                       |
| gpio_pin_sharing    | 1:0  | RW         | 00'b        | GPIO Pin Sharing<br>00: GPIO      01: IRQ_Out<br>10: Reserved      11: PLL_Out |

### 8.31. *Reg-58h: Over-Current Status*

Default: 003Ch

**Table 45. Reg-58h: Over-Current Status**

| Name                | Bits  | Read/Write | Reset State | Description                                                          |
|---------------------|-------|------------|-------------|----------------------------------------------------------------------|
| ovc_micbias1_status | 15    | R          | 0'h         | MICBIAS Over-Current<br>0: Normal 1: Over-current                    |
| Reserved            | 14:13 | R          | 0'h         | Reserved                                                             |
| ovc_clsab           | 12    | R          | 0'h         | Speaker Over-Current Status<br>0: Normal 1: Over-current             |
| ovc_pmos_clsab_P    | 11    | R          | 0'h         | Speaker P side PMOS Over-Current Status<br>0: Normal 1: Over-current |
| ovc_nmos_clsab_P    | 10    | R          | 0'h         | Speaker P side NMOS Over-Current Status<br>0: Normal 1: Over-current |
| ovc_pmos_clsab_N    | 9     | R          | 0'h         | Speaker N side PMOS Over-Current Status<br>0: Normal 1: Over-current |
| ovc_nmos_clsab_N    | 8     | R          | 0'h         | Speaker N side NMOS Over-Current Status<br>0: Normal 1: Over-current |
| Reserved            | 7:0   | R          | 3C'h        | Reserved                                                             |

### 8.32. *Reg-5Ah: Jack Detect Control Register*

Default: 0000h

**Table 46. Reg-5Ah: Jack Detect Control Register**

| Name     | Bits  | Read/Write | Reset State | Description                                                                                                                 |
|----------|-------|------------|-------------|-----------------------------------------------------------------------------------------------------------------------------|
| jd_sel   | 15:14 | RW         | 0'h         | Jack Detect Select<br>00: OFF 01: GPIO<br>10: JD1 11: JD2                                                                   |
| Reserved | 13:12 | RW         | 0'b         | Reserved                                                                                                                    |
| jd_H_Out | 11:8  | RW         | 0'h         | Output Enable When Selected Jack Detect Is 'High'<br>xxx1: Headphone Out xx1x: AUXOUT_L<br>x1xx: AUXOUT_R 1xxx: Speaker Out |
| jd_L_Out | 7:4   | RW         | 0'h         | Output Enable When Selected Jack Detect Is 'Low'<br>xxx1: Headphone Out xx1x: AUXOUT_L<br>x1xx: AUXOUT_R 1xxx: Speaker Out  |
| Reserved | 3:0   | RW         | 0'b         | Reserved                                                                                                                    |

### 8.33. Reg-5Eh: MISC Control

Default: 0000h

**Table 47. Reg-5Eh: MISC Control**

| Name            | Bits | Read/Write | Reset State | Description                                                                                                                                                                |
|-----------------|------|------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| en_vref_fast    | 15   | RW         | 0'b         | Enable Fast Vref<br>0: Enable fast Vref                      1: Disable fast Vref<br><i>Note: To improve PSRR, en_vref_fast should be disabled before playback/record.</i> |
| Reserved        | 14   | RW         | 0'b         | Reserved.<br>Must be kept to 0.                                                                                                                                            |
| ovc_pd_clsab    | 13   | RW         | 0'h         | Speaker Class-AB Over-Current Auto Power Down<br>0:Not Auto                                  1:Auto                                                                        |
| en_ovc_clsab    | 12   | RW         | 0'h         | Speaker Class-AB Over-Current Detect<br>0: Disable                                  1: Enable                                                                              |
| Reserved        | 11   | RW         | 0'h         | Reserved                                                                                                                                                                   |
| en_dp3_hp       | 10   | RW         | 0'h         | Enable Depop Mode 3 of HP_Out<br>0: Disable                                  1: Enable                                                                                     |
| en_dp2_hp       | 9    | RW         | 0'h         | Enable Depop Mode 2 of HP_Out<br>0: Disable                                  1: Enable                                                                                     |
| en_dp1_hp       | 8    | RW         | 0'h         | Enable Depop Mode 1 of HP_Out<br>0: Disable                                  1: Enable                                                                                     |
| Reserved        | 7    | RW         | 0'h         | Reserved                                                                                                                                                                   |
| en_dp3_aux      | 6    | RW         | 0'h         | Enable Depop Mode 3 of AUX_Out<br>0: Disable                                  1: Enable                                                                                    |
| en_dp2_aux      | 5    | RW         | 0'h         | Enable Depop Mode 2 of AUX_Out<br>0: Disable                                  1: Enable                                                                                    |
| en_dp1_aux      | 4    | RW         | 0'h         | Enable Depop Mode 1 of AUX_Out<br>0: Disable                                  1: Enable                                                                                    |
| main_dac_l_mute | 3    | RW         | 0'h         | Mute Main DAC Left Input<br>0: On                                          1: Mute (-∞ dB)                                                                                 |
| main_dac_r_mute | 2    | RW         | 0'h         | Mute Main DAC Right Input<br>0: On                                          1: Mute (-∞ dB)                                                                                |
| Reserved        | 1    | RW         | 0'h         | Reserved                                                                                                                                                                   |
| irqout_inv_ctrl | 0    | RW         | 0'h         | IRQOUT Inverter Control<br>0: Normal                                  1: Invert                                                                                            |

### 8.34. Reg-60h: Stereo and Spatial Effect Block Control

Default: 0497h

**Table 48. Reg-60h: Stereo and Spatial Effect Block Control**

| Name                | Bits | Read/Write | Reset State | Description                                                                                                                                                                                   |
|---------------------|------|------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| spatial_ctrl_enable | 15   | RW         | 0'b         | Spatial Enable<br>0b: Disable (clear internal state)<br>1b: Enable                                                                                                                            |
| apf_en              | 14   | RW         | 0'h         | Enable All Pass Filter APF(z), EN-APF<br>0: Disable (bypass) and reset<br>1: Enable all pass filter. The coefficient a1 is loaded from REG_MX64.[7:0]                                         |
| pseudo_stereo_en    | 13   | RW         | 0'h         | Enable Pseudo Stereo Block, EN-PSB<br>0: Disabled<br>1: Enabled                                                                                                                               |
| en_3d               | 12   | RW         | 0'h         | Enable Stereo Expansion Block , EN-SEB<br>0: Disable<br>1: Enabled. Load 3D Ratio from ratio_parm_3d, and 3D Gain from gain_parm_3d                                                           |
| gain_parm_3d_l      | 11:9 | RW         | 2'h         | 3D Gain Parameter Left (SEG2)<br>000: Gain=1.0                      001: Gain=1.25<br>010: Gain=1.5                     011: Gain=1.75<br>100: Gain=2                        Others: Reserved |
| gain_parm_3d_r      | 8:6  | RW         | 2'h         | 3D Gain Parameter Right (SEG1)<br>000: Gain=1.0                     001: Gain=1.25<br>010: Gain=1.5                     011: Gain=1.75<br>100: Gain=2                        Others: Reserved |
| ratio_parm_3d_l     | 5:4  | RW         | 1'h         | 3D Ratio Parameter Left (DP2)<br>00: Ratio=0.0                      01: Ratio=0.66<br>10:Ratio=1.0                       11:Reserved                                                          |
| ratio_parm_3d_r     | 3:2  | RW         | 1'h         | 3D Ratio Parameter Right (DP1)<br>00: Ratio=0.0                      01: Ratio=0.66<br>10:Ratio=1.0                       11:Reserved                                                         |
| apf_parm_a1         | 1:0  | RW         | 3'h         | All Pass Filter Parameter a1 in 2's Complement 1.7 Format (-1.0~0.99)<br>00: Reserved<br>01: 32kHz sample rate or lower<br>10: 44.1kHz sample rate<br>11: 48kHz sample rate                   |

*Note: Writes to SEGn and DPn will be ignored when the Spatial effect control bit is enabled. This means individual Spatial coefficients cannot be modified when Spatial is enabled.*

### 8.35. Reg-62h: EQ Control

Default: 0000h

**Table 49. Reg-62h: EQ Control**

| Name         | Bits  | Read/Write | Reset State | Description                                                                                          |
|--------------|-------|------------|-------------|------------------------------------------------------------------------------------------------------|
| eq_all_en    | 15    | RW         | 0'b         | EQ Block Control<br>0b: Disable 1b: Enable                                                           |
| eq_HP_F_mode | 14    | RW         | 0'b         | EQ High Frequency Shelving Filter Mode<br>0: High Frequency Shelving Filter<br>1: -20dB/decade (HPF) |
| Reserved     | 13:12 | R          | 0'h         | Reserved                                                                                             |
| Eq_source    | 11    | RW         | 0'b         | EQ Source<br>0: DAC path 1: ADC path                                                                 |
| Reserved     | 10:5  | R          | 00'h        | Reserved                                                                                             |
| eq_hpf_en    | 4     | RW         | 0'b         | EQ High Pass Filter (HPF) Control<br>0: Disabled (bypass) and reset<br>1: Enabled                    |
| eq_bpf3_en   | 3     | RW         | 0'b         | EQ Band-3 (BP3) Control<br>0: Disabled and reset 1: Enabled.                                         |
| eq_bpf2_en   | 2     | RW         | 0'b         | EQ Band-2 (BP2) Control<br>0: Disabled and reset 1: Enabled.                                         |
| eq_bpf1_en   | 1     | RW         | 0'b         | EQ Band-1 (BP1) Control<br>0: Disabled and reset 1: Enabled.                                         |
| eq_lpf_en    | 0     | RW         | 0'b         | EQ Low Pass Filter (LPF) Control<br>0: Disabled and reset 1: Enabled.                                |

### 8.36. Reg-66h: EQ Mode Change Enable

Default: 0000h

**Table 50. Reg-66h: EQ Mode Change Enable**

| Name           | Bits | Read/Write | Reset State | Description                                                          |
|----------------|------|------------|-------------|----------------------------------------------------------------------|
| Reserved       | 15:5 | RW         | 0'h         | Reserved                                                             |
| eq_hpf_chg_en  | 4    | RW         | 0'b         | EQ High Pass Filter (HPF) Mode Change Enable<br>0: Disable 1: Enable |
| eq_bpf3_chg_en | 3    | RW         | 0'b         | EQ Band-3 (BP3) Mode Change Enable<br>0: Disable 1: Enable           |
| eq_bpf2_chg_en | 2    | RW         | 0'b         | EQ Band-2 (BP2) Mode Change Enable<br>0: Disable 1: Enable           |
| eq_bpf1_chg_en | 1    | RW         | 0'b         | EQ Band-1 (BP1) Mode Change Enable<br>0: Disable 1: Enable           |
| eq_lpf_chg_en  | 0    | RW         | 0'b         | EQ Low Pass Filter (LPF) Mode Change Enable<br>0: Disable 1: Enable  |

*Note: To enable an EQ mode change, the driver should set the new EQ parameters (Index00~Index0C) before setting this register to 'Enable'. After the EQ parameter has been changed, the driver should set this register to 'Disable'.*

### 8.37. *Reg-68h: AVC Control*

Default: 000Bh

**Table 51. Reg-68h: AVC Control**

| Name                | Bits | Read/Write | Reset State | Description                                                                                                                                                                                                                                                                                                         |
|---------------------|------|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| avc_en              | 15   | RW         | 0'b         | Auto Volume Control (AVC) Enable<br>0: Disable AVC                      1: Enable AVC                                                                                                                                                                                                                               |
| avc_ref_ch          | 14   | RW         | 0'b         | AVC Reference Channel Selection<br>0: Left Channel                      1: Right Channel                                                                                                                                                                                                                            |
| Nonact_reg_action   | 13   | RW         | 0'b         | Gain Action of Non-Active Region<br>0: Keep Previous Gain              1: Unit Gain                                                                                                                                                                                                                                 |
| Nonact_feedback_sel | 12   | RW         | 0'b         | Non-Active Threshold Gain Feedback Selection<br>0: No gain feedback              1: Gain feedback                                                                                                                                                                                                                   |
| Reserved            | 11:5 | RW         | 0'h         | Reserved                                                                                                                                                                                                                                                                                                            |
| monitor_window      | 4:0  | RW         | 0B'h        | Monitor Window Control (Unit: 2 <sup>(n+1)</sup> samples)<br>(default:01011b)<br>00000b: 2 <sup>(1)</sup> sample              00001b: 2 <sup>(2)</sup> samples<br>00010b: 2 <sup>(3)</sup> samples              10000b: 2 <sup>(17)</sup> samples<br>Others: Reserved.<br>Maximum=10000000000000000=2 <sup>17</sup> |

### 8.38. *Reg-6Ah: Index Address*

Default: 0000h

**Table 52. Reg-6Ah: Index Address**

| Name       | Bits | Read/Write | Reset State | Description   |
|------------|------|------------|-------------|---------------|
| Reserved   | 15:7 | R          | 0'h         | Reserved      |
| index_addr | 6:0  | RW         | 0'h         | Index Address |

### 8.39. *Reg-6Ch: Index Data*

Default: 0000h

**Table 53. Reg-6Ch: Index Data**

| Name       | Bits | Read/Write | Reset State | Description |
|------------|------|------------|-------------|-------------|
| index_data | 15:0 | RW         | 0'h         | Index Data  |

### 8.40. *Index-00h: EQ Band-0 Coefficient (LP0: a1)*

Default: 0000h

**Table 54. Index-00h: EQ Band-0 Coefficient (LP0: a1)**

| Bit  | Type | Function                                                                                |
|------|------|-----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 formats (The range is from -4~3.99, the a1 should be in -2~1.99) |

*Note: For low pass filter for Bass control – LP0 has filter coefficient a1 and gain Ho must be set (see Table 55).*

### 8.41. *Index-01h: EQ Band-0 Gain (LP0: Ho)*

Default: 0000h

**Table 55. Index-01h: EQ Band-0 Gain (LP0: Ho)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -4~3.99) |

### 8.42. *Index-02h: EQ Band-1 Coefficient (BP1: a1)*

Default: 0000h

**Table 56. Index-02h: EQ Band-1 Coefficient (BP1: a1)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2~1.99) |

### 8.43. *Index-03h: EQ Band-1 Coefficient (BP1: a2)*

Default: 0000h

**Table 57. Index-03h: EQ Band-1 Coefficient (BP1: a2)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2~1.99) |

### 8.44. *Index-04h: EQ Band-1 Gain (BP1: Ho)*

Default: 0000h

**Table 58. Index-04h: EQ Band-1 Gain (BP1: Ho)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -4~3.99) |

### 8.45. *Index-05h: EQ Band-2 Coefficient (BP2: a1)*

Default: 0000h

**Table 59. Index-05h: EQ Band-2 Coefficient (BP2: a1)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2~1.99) |

### 8.46. *Index-06h: EQ Band-2 Coefficient (BP2: a2)*

Default: 0000h

**Table 60. Index-06h: EQ Band-2 Coefficient (BP2: a2)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a2 should be in -2~1.99) |

### 8.47. *Index-07h: EQ Band-2 Gain (BP2: Ho)*

Default: 0000h

**Table 61. Index-07h: EQ Band-2 Gain (BP2: Ho)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -4~3.99) |

### 8.48. *Index-08h: EQ Band-3 Coefficient (BP3: a1)*

Default: 0000h

**Table 62. Index-08h: EQ Band-3 Coefficient (BP3: a1)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2~1.99) |

### 8.49. *Index-09h: EQ Band-3 Coefficient (BP3: a2)*

Default: 0000h

**Table 63. Index-09h: EQ Band-3 Coefficient (BP3: a2)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a2 should be in -2~1.99) |

### 8.50. *Index-0Ah: EQ Band-3 Gain (BP3: Ho)*

Default: 0000h

**Table 64. Index-0Ah: EQ Band-3 Gain (BP3: Ho)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -4~3.99) |

### 8.51. *Index-0Bh: EQ Band-4 Coefficient (HPF: a1)*

Default: 0000h

**Table 65. Index-0Bh: EQ Band-4 Coefficient (HPF: a1)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the a1 should be in -2~1.99) |

### 8.52. *Index-0Ch: EQ Band-4 Gain (HPF: Ho)*

Default: 0000h

**Table 66. Index-0Ch: EQ Band-4 Gain (HPF: Ho)**

| Bit  | Type | Function                                                                               |
|------|------|----------------------------------------------------------------------------------------|
| 15:0 | RW   | 2's complement in 3.13 format (The range is from -4~3.99, the Ho should be in -2~1.99) |

### 8.53. *Index-11h: EQ Input Volume Control*

Default: 0000h

**Table 67. Index-11h: EQ Input Volume Control**

| Bit  | Type | Function                                                                                     |
|------|------|----------------------------------------------------------------------------------------------|
| 15:2 | -    | Reserved                                                                                     |
| 1:0  | RW   | 7-Bit Volume Unsigned Ratio EQIn-VOL-LR<br>00b: 0dB<br>01b: -6dB<br>10b: -12dB<br>11b: -18dB |

### 8.54. *Index-12h: EQ Output Volume Control*

Default: 0001h

**Table 68. Index-12h: EQ Output Volume Control**

| Bit  | Type | Function                                                                                                                                                         |
|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | -    | Reserved                                                                                                                                                         |
| 2:0  | RW   | 7-Bit Volume Unsigned Ratio EQOut-VOL-LR<br>000b: -3dB      001b: 0dB      010b: 3dB      011b: 6dB<br>100b: 9dB      101b: 12dB      110b: 15dB      111b: 18dB |

### 8.55. *Index-21h: Auto Volume Control Register 1*

Default: 0400h

**Table 69. Index-21h: Auto Volume Control Register 1**

| Bit  | Type | Function                                                                |
|------|------|-------------------------------------------------------------------------|
| 15   | -    | Reserved                                                                |
| 14:0 | RW   | The Maximum PCM absolute level after AVC, Thmax (=0~2 <sup>15</sup> -1) |

### 8.56. *Index-22h: Auto Volume Control Register 2*

Default: 0390h

**Table 70. Index-22h: Auto Volume Control Register 2**

| Bit  | Type | Function                                                                |
|------|------|-------------------------------------------------------------------------|
| 15   | -    | Reserved                                                                |
| 14:0 | RW   | The Minimum PCM absolute level after AVC, Thmin (=0~2 <sup>15</sup> -1) |

### 8.57. *Index-23h: Auto Volume Control Register 3*

Default: 0001h

**Table 71. Index-23h: Auto Volume Control Register 3**

| Bit  | Type | Function                                                                                           |
|------|------|----------------------------------------------------------------------------------------------------|
| 15   | -    | Reserved                                                                                           |
| 14:0 | RW   | The Non-active PCM absolute level AVC will keep analog unit gain, Thnonact (=0~2 <sup>15</sup> -1) |

*Note: Initial Index23=0001'h*

## 8.58. Index-24h: Auto Volume Control Register 4

Default: 01FFh

**Table 72. Index-24h: Auto Volume Control Register 4**

| Bit  | Type | Function                                                                                                                                                          |
|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RW   | CNTMAXTH1. Controls the Sensitivity to Increased Gain (unit:2 <sup>1</sup> )<br>This value should be less than CNTMAXTH2 (Max=111111111111110=2 <sup>18-2</sup> ) |

## 8.59. Index-25h: Auto Volume Control Register 5

Default: 0200h

**Table 73. Index-25h: Auto Volume Control Register 5**

| Bit  | Type | Function                                                                                                                                                                                                 |
|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RW   | CNTMAXTH2. Controls the Sensitivity to Decreased Gain (unit:2 <sup>1</sup> )<br>This value should be less than Monitor Window (Optimal: 1/2 Monitor Window)<br>(Max=1111111111111110=2 <sup>18-2</sup> ) |

Note: CNTMAXTH1 < CNTMAXTH2

## 8.60. Index-39h: Digital Internal Register

Default: 9800h

**Table 74. Index-39h: Digital Internal Register**

| Bit   | Type | Function                                                   |
|-------|------|------------------------------------------------------------|
| 15    | RW   | Pad Drive Capability<br>0b: Weak drive<br>1b: Strong drive |
| 14:13 | RW   | Reserved                                                   |
| 12    | RW   | Power Gating Enable<br>0: Disable<br>1: Enable             |
| 11    | RW   | Vref Power Control Enable<br>0: Enable<br>1: Disable       |
| 10:0  | RW   | Reserved                                                   |

## 8.61. *Index-46h: Class-D Internal Register*

Default: CF00h

**Table 75. Index-46h: Class-D Internal Register**

| Bit   | Type | Function                |               |             |
|-------|------|-------------------------|---------------|-------------|
| 15    | RW   | Class-D Speaker (pos)   | 0: Power down | 1: Power on |
| 14    | RW   | Class-D Speaker (neg)   | 0: Power down | 1: Power on |
| 13:12 | R    | Reserved                |               |             |
| 11    | RW   | Class-D VREF Generator  | 0: Power down | 1: Power on |
| 10    | RW   | Class-D Ramp Generator  | 0: Power down | 1: Power on |
| 9     | RW   | Class-D Clock Generator | 0: Power down | 1: Power on |
| 8     | RW   | Class-D BIAS Generator  | 0: Power down | 1: Power on |
| 7:0   | R    | Reserved                |               |             |

## 8.62. *Reg-7Ch: VENDOR ID 1*

Default: 10ECh

**Table 76. Reg-7Ch: VENDOR ID 1**

| Name       | Bits | Read/Write | Reset State | Description    |
|------------|------|------------|-------------|----------------|
| vender_id1 | 15:0 | R          | 10EC'h      | Vendor ID=10EC |

## 8.63. *Reg-7Eh: VENDOR ID 2*

Default: 2003h

**Table 77. Reg-7Eh: VENDOR ID 2**

| Name       | Bits | Read/Write | Reset State | Description   |
|------------|------|------------|-------------|---------------|
| vender_id  | 15:8 | R          | 10'h        | Device ID=21  |
| device_id2 | 7:0  | R          | 03'h        | Version ID=03 |

## 9. Electrical Characteristics

### 9.1. DC Characteristics

#### 9.1.1. Absolute Maximum Ratings

**Table 78. Absolute Maximum Ratings**

| Parameter                     | Symbol | Min  | Typ | Max  | Units |
|-------------------------------|--------|------|-----|------|-------|
| Power Supplies                |        |      |     |      |       |
| Digital IO Buffer             | DBVDD  | -0.3 | -   | 3.63 | V     |
| Digital Core                  | DCVDD  | -0.3 | -   | 3.63 | V     |
| Analog                        | AVDD   | -0.3 | -   | 3.63 | V     |
| Speaker                       | SPKVDD | -0.3 | -   | 7    | V     |
| Operating Ambient Temperature | Ta     | -25  | -   | +85  | °C    |
| Storage Temperature           | Ts     | -55  | -   | +125 | °C    |

#### 9.1.2. Recommended Operating Conditions

**Table 79. Recommended Operating Conditions**

| Parameter         | Symbol  | Min  | Typ | Max | Units |
|-------------------|---------|------|-----|-----|-------|
| Digital IO Buffer | DBVDD   | 1.71 | 3.3 | 3.6 | V     |
| Digital Core      | DCVDD   | 1.71 | 3.3 | 3.6 | V     |
| Analog            | AVDD    | 2.3  | 3.3 | 3.6 | V     |
| Speaker           | SPKVDD* | 2.3  | 3.3 | 5   | V     |

Note: '\*' indicates a 10μF Capacitor must be connected from SPKVDD to SPKGND, and should be placed as close as possible to the SPKVDD pin of the ALC5621.

#### 9.1.3. Static Characteristics

**Table 80. Static Characteristics**

| Parameter                 | Symbol          | Min      | Typ | Max       | Units |
|---------------------------|-----------------|----------|-----|-----------|-------|
| Input Voltage Range       | V <sub>IN</sub> | -0.30    | -   | DVDD+0.30 | V     |
| Low Level Input Voltage   | V <sub>IL</sub> | -        | -   | 0.35DVDD  | V     |
| High Level Input Voltage  | V <sub>IH</sub> | 0.65DVDD | -   | -         | V     |
| High Level Output Voltage | V <sub>OH</sub> | 0.9DVDD  | -   | -         | V     |
| Low Level Output Voltage  | V <sub>OL</sub> | -        | -   | 0.1DVDD   | V     |

Note: DVDD=3.3V, T<sub>ambient</sub>=25 °C, with 50pF external load.

## 9.2. Analog Performance Characteristics

**Table 81. Analog Performance Characteristics**

| Parameter                                                                       | Min  | Typ | Max   | Units      |
|---------------------------------------------------------------------------------|------|-----|-------|------------|
| Full Scale Input Voltage                                                        |      |     |       |            |
| Line Inputs                                                                     | -    | 1.0 | -     | Vrms       |
| MIC Inputs (Non-Boost)                                                          | -    | 1.0 | -     | Vrms       |
| MIC Inputs (Boost 20dB)                                                         | -    | 0.1 | -     | Vrms       |
| ADC                                                                             | -    | 0.7 | -     | Vrms       |
| Full Scale Output Voltage                                                       |      |     |       |            |
| MONO Outputs                                                                    | -    | 1.0 | -     | Vrms       |
| Headphone Amplifiers Outputs                                                    | -    | 1.0 | -     | Vrms       |
| Speaker Amplifiers Outputs                                                      | -    | 1.5 | -     | Vrms       |
| DAC                                                                             | -    | 1.0 | -     | Vrms       |
| S/N Ratio (A-Weighted, HPL/R or MONO with 10K $\Omega$ /50pF Load)              |      |     |       |            |
| STEREO DAC                                                                      | -    | 92  | -     | dB         |
| STEREO ADC                                                                      | -    | 85  | -     | dB         |
| Total Harmonic Distortion+Noise<br>(HPL/R or MONO with 10K $\Omega$ /50pF Load) |      |     |       |            |
| STEREO DAC                                                                      | -    | -85 | -     | dB         |
| STEREO ADC                                                                      | -    | -80 | -     | dB         |
| MIC Boost Amplifier                                                             |      |     |       |            |
| Gain=20dB                                                                       | -    | 20  | -     | dB         |
| Gain=30dB                                                                       | -    | 30  | -     | dB         |
| Input Impedance (Gain=0dB, ADC mixer=On/Off)                                    |      |     |       |            |
| MIC1N, MIC2N (Differential Mode)                                                | -    | 16  | -     | K $\Omega$ |
| MIC1P, MIC2P                                                                    | -    | 16  | -     | K $\Omega$ |
| Input Impedance (Gain=0dB, ADC Mixer=On)                                        |      |     |       |            |
| LINE_IN_L/R, AUXIN_L/R                                                          | 12.8 | 16  | 19.2  | K $\Omega$ |
| Input Impedance (Gain=0dB, ADC Mixer=Off)                                       |      |     |       |            |
| LINE_IN_L/R, AUXIN_L/R                                                          | 25.6 | 32  | 38.4  | K $\Omega$ |
| MONO_OUT/AUXOUT_L/R Amplifier Quiescent Current<br>(32 $\Omega$ Load)           | -    | 900 | -     | $\mu$ A    |
| MONO_OUT/AUXOUT_L/R Amplifier Efficiency<br>(fIN=1KHz, 32 $\Omega$ Load)        |      |     |       |            |
| Single-Ended Mode (Output Power=25mW)                                           | 50   | -   | -     | %          |
| BTL Mode (Output Power=75mW)                                                    | 50   | -   | -     | %          |
| MONO_OUT/AUXOUT_L/R Amplifier THD+N                                             |      |     |       |            |
| Single-Ended Mode (10K $\Omega$ Load)                                           |      |     |       |            |
| Output Power=0.1mW                                                              | -    | -85 | -     | dB         |
| BTL Mode (10K $\Omega$ Load)                                                    |      |     |       |            |
| Output Power=0.1mW                                                              | -    | -85 | -     | dB         |
| Headphone Amplifier Output Power (32 $\Omega$ Load)                             | -    | -   | 31.25 | mW         |
| MONO_OUT/AUXOUT_L/R Amplifier PSRR (217Hz)                                      | -    | 50  | -     | dB         |

| Parameter                                                                                | Min | Typ  | Max | Units |
|------------------------------------------------------------------------------------------|-----|------|-----|-------|
| Headphone Amplifier Efficiency<br>(f <sub>IN</sub> =1KHz, 32Ω Load, Output Power=25mW)   | 50  | -    | -   | %     |
| Headphone Amplifier THD+N (32Ω Load)                                                     |     |      |     |       |
| Output Power=20mW                                                                        | -   | -75  | -   | dB    |
| Output Power=25mW                                                                        | -   | -74  | -   | dB    |
| Headphone Amplifier PSRR (217Hz)                                                         | -   | 50   | -   | dB    |
| BTL Class-D Speaker Amplifier Output Power (4Ω Load)                                     |     |      |     |       |
| @4.2V with THD+N=40dB                                                                    | -   | 1200 | -   | mW    |
| @5V with THD+N=40dB                                                                      | -   | 1800 | -   | mW    |
| @4.2V with THD+N=20dB                                                                    | -   | 1800 | -   | mW    |
| @5V with THD+N=20dB                                                                      | -   | 2600 | -   | mW    |
| BTL Class-D Speaker Amplifier Output Power (8Ω Load)                                     |     |      |     |       |
| @4.2V with THD+N=40dB                                                                    | -   | 700  | -   | mW    |
| @5V with THD+N=40dB                                                                      | -   | 1050 | -   | mW    |
| @4.2V with THD+N=20dB                                                                    | -   | 1000 | -   | mW    |
| @5V with THD+N=20dB                                                                      | -   | 1500 | -   | mW    |
| BTL Class-AB Speaker Amplifier Output Power (4Ω Load)                                    |     |      |     |       |
| @4.2V with THD+N=40dB                                                                    | -   | 1100 | -   | mW    |
| @5V with THD+N=40dB                                                                      | -   | 1700 | -   | mW    |
| @4.2V with THD+N=20dB                                                                    | -   | 1700 | -   | mW    |
| @5V with THD+N=20dB                                                                      | -   | 2600 | -   | mW    |
| BTL Class-AB Speaker Amplifier Output Power (8Ω Load)                                    |     |      |     |       |
| @4.2V with THD+N=40dB                                                                    | -   | 650  | -   | mW    |
| @5V with THD+N=40dB                                                                      | -   | 1050 | -   | mW    |
| @4.2V with THD+N=20dB                                                                    | -   | 900  | -   | mW    |
| @5V with THD+N=20dB                                                                      | -   | 1350 | -   | mW    |
| BTL Speaker Amplifier Efficiency<br>(f <sub>IN</sub> =1KHz, 8Ω Load, Output Power=900mW) |     |      |     |       |
| Class-AB                                                                                 | 50  | -    | -   | %     |
| Class-D                                                                                  | -   | 82   | -   | %     |
| BTL Speaker Amplifier THD+N                                                              |     |      |     |       |
| Class-AB_Strong (8Ω Load)                                                                |     |      |     |       |
| Output Power=350mW                                                                       | -   | -80  | -   | dB    |
| Output Power=700mW                                                                       | -   | -75  | -   | dB    |
| Class-D (8Ω Load)                                                                        |     |      |     |       |
| Output Power=350mW                                                                       | -   | -80  | -   | dB    |
| Output Power=700mW                                                                       | -   | -70  | -   | dB    |
| BTL Speaker Amplifier THD+N                                                              |     |      |     |       |
| Class-AB_Weak (10KΩ/50pF Load)                                                           | -   | -85  | -   | dB    |
| BTL Speaker Amplifier SNR                                                                |     |      |     |       |
| Class-AB_Weak (10KΩ/50pF Load)                                                           | -   | -90  | -   | dB    |
| BTL Speaker Amplifier PSRR (217Hz)                                                       | -   | 50   | -   | dB    |

| Parameter                                                | Min | Typ   | Max | Units |
|----------------------------------------------------------|-----|-------|-----|-------|
| Quiescent Playback Current (DAC to HP_OUT with 16Ω Load) |     |       |     |       |
| IDDA (Analog Block)                                      | -   | -     | 3.9 | mA    |
| IDDD (Digital Block)                                     | -   | -     | 5.4 | mA    |
| Power Down Current                                       |     |       |     |       |
| IDDA (Analog Block)                                      | -   | -     | 10  | μA    |
| IDDD (Digital Block)                                     | -   | -     | 1   | μA    |
| MICBIAS Output Voltage                                   |     |       |     |       |
| 0.75*AVDD Setting                                        | -   | 2.475 | -   | V     |
| 0.9*AVDD Setting                                         | -   | 2.97  | -   | V     |
| MICBIAS Drive Current                                    | 2   | -     | 3   | mA    |

*Note: Standard test conditions*

$T_{ambient}=25\text{ }^{\circ}\text{C}$ ,  $DBVDD=DCVDD=AVDD=3.3\text{V}$ ,  $SPKVDD=5\text{V}$

$1\text{kHz}$  input sine wave; PCM Sampling frequency= $48\text{kHz}$ ;  $0\text{dB}=1\text{Vrms}$ , Test bench Characterization BW:  $10\text{Hz}\sim 22\text{kHz}$ ,  $0\text{dB}$  attenuation; EQ and 3D disabled.

## 9.3. Signal Timing

### 9.3.1. I<sup>2</sup>C Control Interface

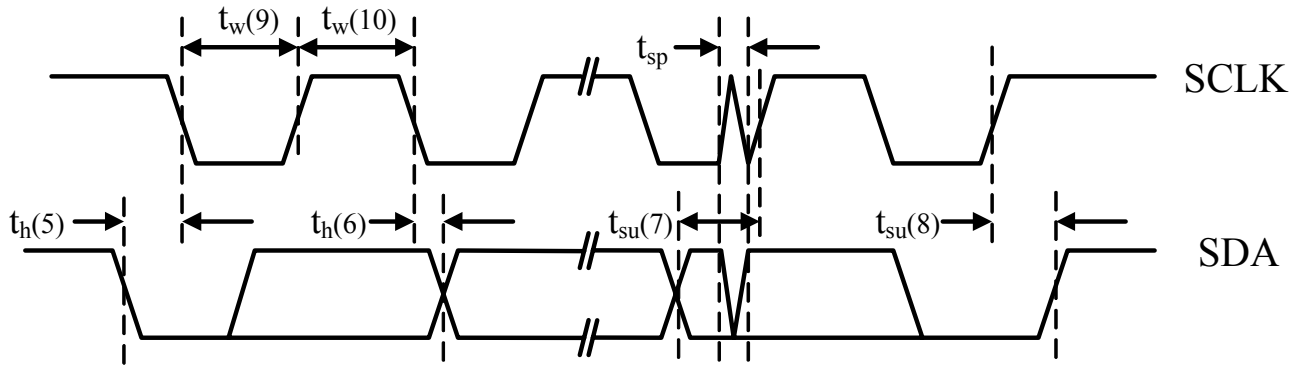


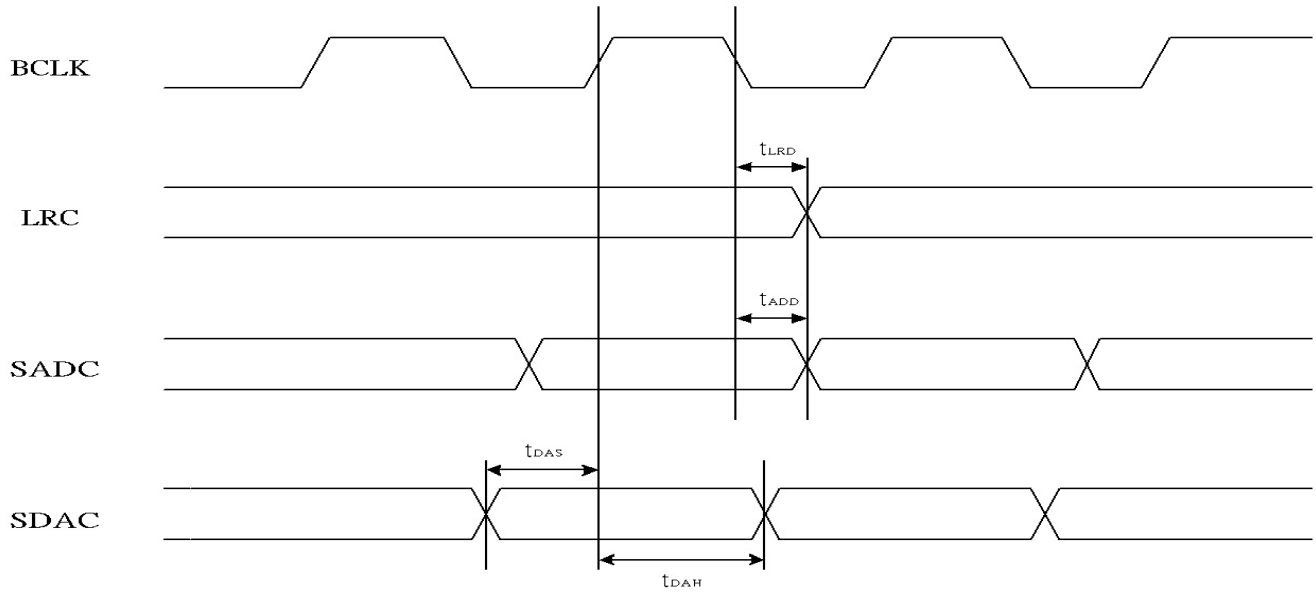
Figure 21. I<sup>2</sup>C Control Interface

Table 82. I<sup>2</sup>C Timing

| Parameter                                     | Symbol      | Min | Typ | Max  | Units   |
|-----------------------------------------------|-------------|-----|-----|------|---------|
| Clock Pulse Duration                          | $t_w(9)$    | 1.3 | -   | -    | $\mu$ s |
| Clock Pulse Duration                          | $t_w(10)$   | 600 | -   | -    | ns      |
| Clock Frequency                               | f           | 0   | -   | 400K | Hz      |
| Start Hold Time                               | $t_h(5)$    | 600 | -   | -    | ns      |
| Data Setup Time                               | $t_{su}(7)$ | 100 | -   | -    | ns      |
| Data Hold Time                                | $t_h(6)$    | -   | -   | 900  | ns      |
| Rising Time                                   | $t_r$       | -   | -   | 300  | ns      |
| Falling Time                                  | $t_f$       | -   | -   | 300  | ns      |
| Stop Setup Time                               | $t_{su}(8)$ | 600 | -   | -    | ns      |
| Pulse Width of Spikes Suppressed Input Filter | $t_{sp}$    | 0   | -   | 50   | ns      |

Note: Condition: MCLK > 8MHz.

### 9.3.2. I<sup>2</sup>S/PCM Interface Master Mode

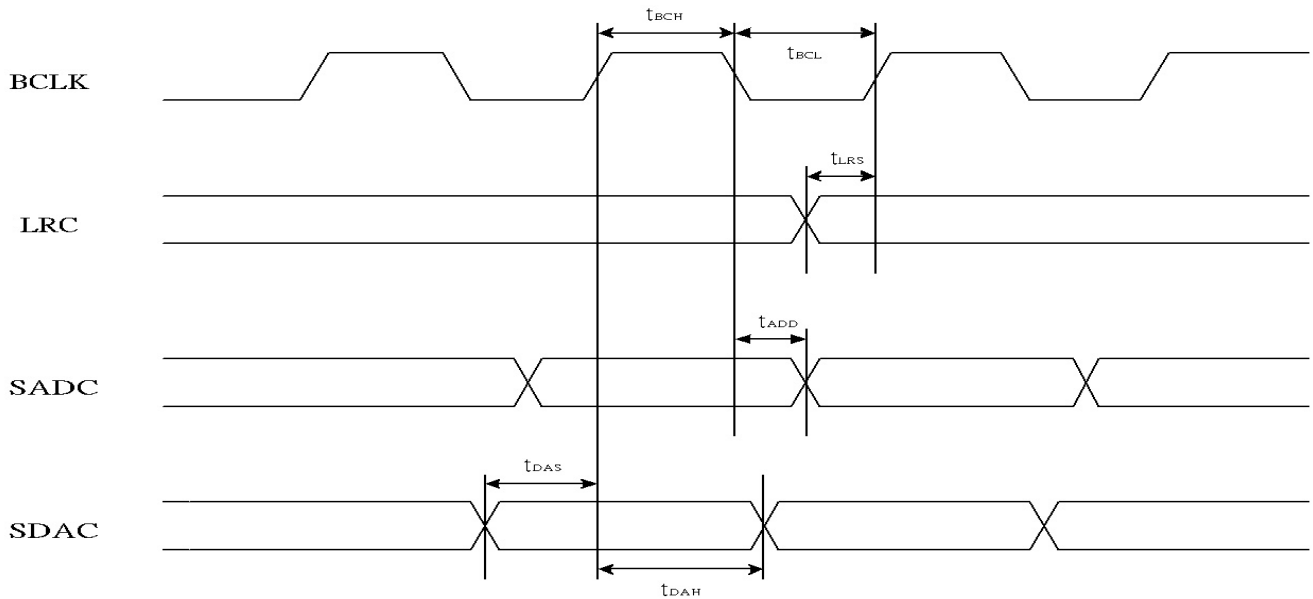


**Figure 22. Timing of I<sup>2</sup>S/PCM Master Mode**

**Table 83. Timing of I<sup>2</sup>S/PCM Master Mode**

| Parameter                 | Symbol    | Min | Typ | Max | Units |
|---------------------------|-----------|-----|-----|-----|-------|
| LRCK Output to BCLK Delay | $t_{LRD}$ | -   | -   | 30  | ns    |
| Data Output to BCLK Delay | $t_{ADD}$ | -   | -   | 30  | ns    |
| Data Input Setup Time     | $t_{DAS}$ | 10  | -   | -   | ns    |
| Data Input Hold Time      | $t_{DAH}$ | 10  | -   | -   | ns    |

### 9.3.3. I<sup>2</sup>S/PCM Interface Slave Mode



**Figure 23. I<sup>2</sup>S/PCM Slave Mode Timing**

**Table 84. I<sup>2</sup>S/PCM Slave Mode Timing**

| Parameter                 | Symbol    | Min | Typ | Max | Units |
|---------------------------|-----------|-----|-----|-----|-------|
| BCLK High Pulse Width     | $t_{BCH}$ | 20  | -   | -   | ns    |
| BCLK Low Pulse Width      | $t_{BCL}$ | 20  | -   | -   | ns    |
| LRCK Input Setup Time     | $t_{LRS}$ | 30  | -   | -   | ns    |
| Data Output to BCLK Delay | $t_{ADD}$ | -   | -   | 30  | ns    |
| Data Input Setup Time     | $t_{DAS}$ | 10  | -   | -   | ns    |
| Data Input Hold Time      | $t_{DAH}$ | 10  | -   | -   | ns    |

**BTL Input**

**BTL Output**

**Single End Input**

**Single End Output**

**NOTE: For SPKVD by pass cap, C2 > 10u is necessary**

**GND**

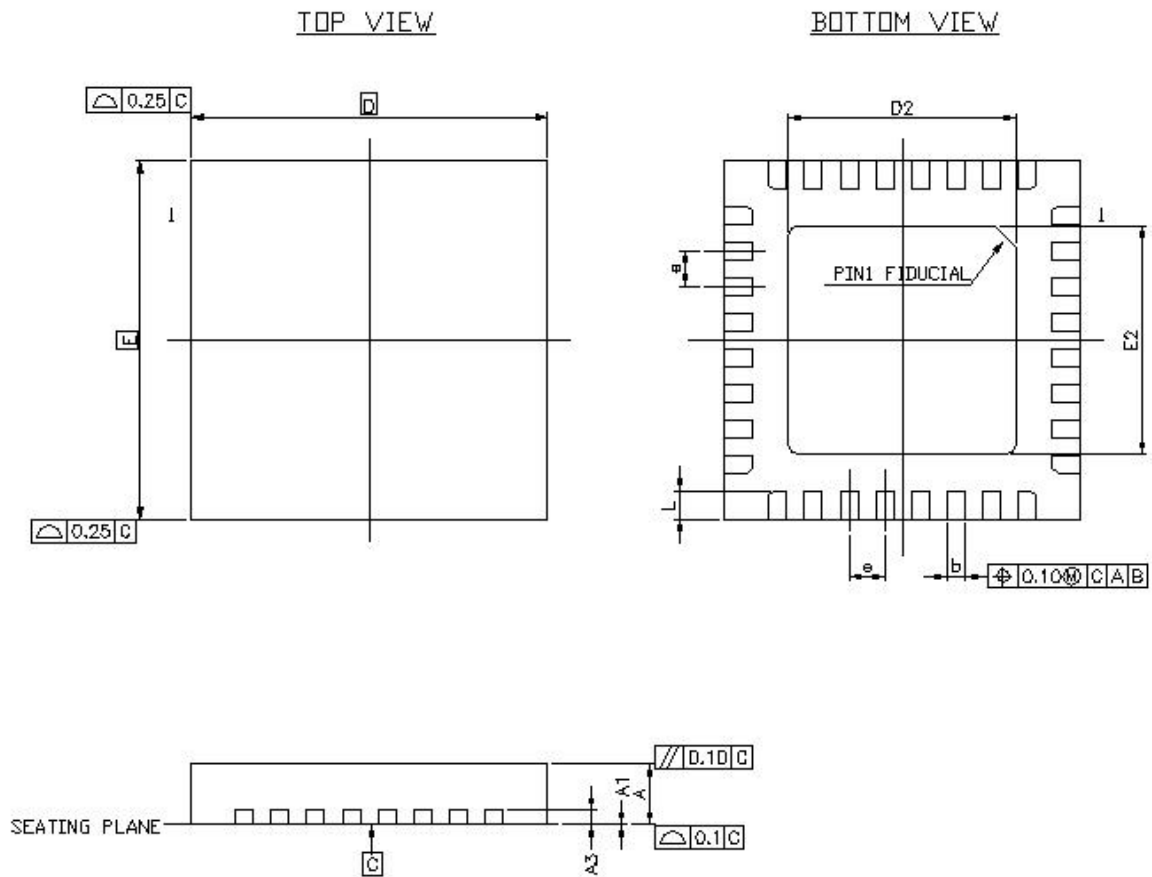
**OSC**

**ALC5621**

**OSC 24 SWAVE**

# 11. Mechanical Dimensions

## Plastic Quad Flat No-Lead Package 32 Leads 5x5mm Outline



| Symbol                         | Dimension in mm |      |      | Dimension in inch |       |       |
|--------------------------------|-----------------|------|------|-------------------|-------|-------|
|                                | Min             | Nom  | Max  | Min               | Nom   | Max   |
| A                              | 0.75            | 0.85 | 1.00 | 0.030             | 0.034 | 0.039 |
| A <sub>1</sub>                 | 0.00            | 0.02 | 0.05 | 0.000             | 0.001 | 0.002 |
| A <sub>3</sub>                 | 0.20REF         |      |      | 0.008REF          |       |       |
| b                              | 0.18            | 0.25 | 0.30 | 0.007             | 0.010 | 0.012 |
| c                              | -               | -    | 0.6  | -                 | -     | 0.024 |
| D/E                            | 5.00BSC         |      |      | 0.197BSC          |       |       |
| D <sub>2</sub> /E <sub>2</sub> | 3.10            | 3.35 | 3.60 | 0.122             | 0.132 | 0.142 |
| e                              | 0.50BSC         |      |      | 0.020BSC          |       |       |
| L                              | 0.30            | 0.40 | 0.50 | 0.012             | 0.016 | 0.020 |

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

## 12. Appendix A: Stereo I<sup>2</sup>S Clock Table

| MCLK<br>(Hz) | PLL Output<br>(Hz) | Sel_sysclk | DA/AD Clock |           | DAC/ADC Sample Rate<br>LRCK (Hz) |       |
|--------------|--------------------|------------|-------------|-----------|----------------------------------|-------|
|              |                    | Reg42[15]  | Reg36       |           |                                  |       |
|              |                    |            | BCLK=64fs   | BCLK=32fs |                                  |       |
| 24576000     | X                  | 0'b        | 0x386F      | 0x3C6B    | 8000                             |       |
| X            | 24576000           | 1'b        |             |           |                                  |       |
| 16384000     | X                  | 0'b        | 0x366D      | 0x3A69    |                                  | 12000 |
| X            | 16384000           | 1'b        |             |           |                                  |       |
| 24576000     | X                  | 0'b        | 0x366D      | 0x3A69    | 16000                            |       |
| X            | 24576000           | 1'b        |             |           |                                  |       |
| 18432000     | X                  | 0'b        | 0x286F      | 0x2C6B    |                                  | 24000 |
| X            | 18432000           | 1'b        |             |           |                                  |       |
| 24576000     | X                  | 0'b        | 0x286F      | 0x2C6B    | 32000                            |       |
| X            | 24576000           | 1'b        |             |           |                                  |       |
| 16384000     | X                  | 0'b        | 0x266D      | 0x2A69    |                                  | 48000 |
| X            | 16384000           | 1'b        |             |           |                                  |       |
| 24576000     | X                  | 0'b        | 0x266D      | 0x2A69    | 11025                            |       |
| X            | 24576000           | 1'b        |             |           |                                  |       |
| 18432000     | X                  | 0'b        | 0x186F      | 0x1C6B    |                                  | 22050 |
| X            | 18432000           | 1'b        |             |           |                                  |       |
| 24576000     | X                  | 0'b        | 0x186F      | 0x1C6B    | 44100                            |       |
| X            | 24576000           | 1'b        |             |           |                                  |       |
| 16384000     | X                  | 0'b        | 0x166D      | 0x1A69    |                                  | 8000  |
| X            | 16384000           | 1'b        |             |           |                                  |       |
| 24576000     | X                  | 0'b        | 0x166D      | 0x1A69    | 12000                            |       |
| X            | 24576000           | 1'b        |             |           |                                  |       |
| 18432000     | X                  | 0'b        | 0x086F      | 0x0C6B    |                                  | 16000 |
| X            | 18432000           | 1'b        |             |           |                                  |       |
| 22579200     | X                  | 0'b        | 0x366D      | 0x3A69    | 24000                            |       |
| X            | 22579200           | 1'b        |             |           |                                  |       |
| 16934400     | X                  | 0'b        | 0x286F      | 0x2C6B    |                                  | 32000 |
| X            | 16934400           | 1'b        |             |           |                                  |       |
| 22579200     | X                  | 0'b        | 0x266D      | 0x2A69    | 44100                            |       |
| X            | 22579200           | 1'b        |             |           |                                  |       |
| 16934400     | X                  | 0'b        | 0x186F      | 0x1C6B    |                                  | 8000  |
| X            | 16934400           | 1'b        |             |           |                                  |       |
| 22579200     | X                  | 0'b        | 0x166D      | 0x1A69    | 12000                            |       |
| X            | 22579200           | 1'b        |             |           |                                  |       |
| 16934400     | X                  | 0'b        | 0x086F      | 0x0C6B    |                                  | 16000 |
| X            | 16934400           | 1'b        |             |           |                                  |       |

## 13. Ordering Information

**Table 85. Ordering Information**

| Part Number | Package                                 | Status          |
|-------------|-----------------------------------------|-----------------|
| ALC5621-GR  | QFN-32 in 'Green' Package (Tray)        | Mass Production |
| ALC5621-GRT | QFN-32 in 'Green' Package (Tape & Reel) | Mass Production |

*Note 1: See page 6 for Green package and version identification.*

*Note 2: Above parts are tested under AVDD=SPKVDD=3.3V.*

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