RTL8812AU-CG

SINGLE-CHIP IEEE 802.11ac 2T2R WLAN CONTROLLER WITH USB 2.0/3.0 INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.2	24, May, 2012	Preliminary release.

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8812AU-CG is a highly integrated single-chip MIMO (Multiple In, Multiple Out) Wireless LAN (WLAN) USB 2.0/3.0 network interface controller complying with the wireless very high throughput IEEE 802.11ac Draft 2.0 and 802.11n specifications. The RTL8812AU-CG provides a complete solution for a high-performance wireless client and also supports WiFi Direct feature that can easily build a WiFi P2P PAN network.

The RTL8812AU-CG baseband implements Multiple Input, Multiple Output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Features include two spatial stream transmissions, short Guard Interval (GI) of 400ns, spatial spreading, and support for both 20MHz, 40MHz and 80MHz channel bandwidth. Moreover, RTL8812AU provides one spatial stream space-time block code (STBC) , Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8812AU also supports explicit sounding packet feedback that helps senders with beamforming capability. With 2 independent RF blocks, the RTL8812AU can perform fast roaming without link interruption.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 866.7Mbps for IEEE 802.11ac MIMO OFDM.

The RTL8812AU-CG builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with Maximal-Ratio-Combine (MRC) applying up to two receive paths is implemented. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8812AU-CG supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8812AU-CG MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac Draft 2.0 for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8812AU-CG provides simple legacy, 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- QFN76 9x9mm package
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac Draft 2.0 compatible WLAN
- 802.11ac MIMO solution for 5G band
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- 2x2 MIMO technology for extended reception robustness and exceptional throughput
- Maximum PHY data rate up to 173.3 Mbps using 20MHz bandwidth, 400Mbps using 40MHz bandwidth, and 866.7Mbps using 80MHz bandwidth.
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

Host Interface

- Complies with USB Specification Revision 3.0

Standards Supported

- IEEE 802.11a/b/g/n/ac Draft 2.0 compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.
- Cisco Compatible Extensions (CCX) for WLAN devices

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8812AU-CG to assume multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications.

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- CCA on secondary through RTS/CTS handshake.

- Support TCP/UDP/IP checksum offload

Peripheral Interfaces

- Up to 12 General Purpose Input/Output pins
- Three configurable LED pins (mux with GPIO pins)
- Configurable Bluetooth Coexistence Interface (mux with GPIO pins)
- Generates 40MHz clock for peripheral chip.
- Single external power source 3.3V only

PHY Features

- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- Short Guard Interval (400ns)
- Sounding packet.
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7Mbps in 802.11ac.
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK
- Support STBC
- Support LDPC
- Hardware antenna diversity
- Selectable digital transmit and receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

3. Application Diagrams

3.1. 11ac Dual-Band 2x2 RF Application

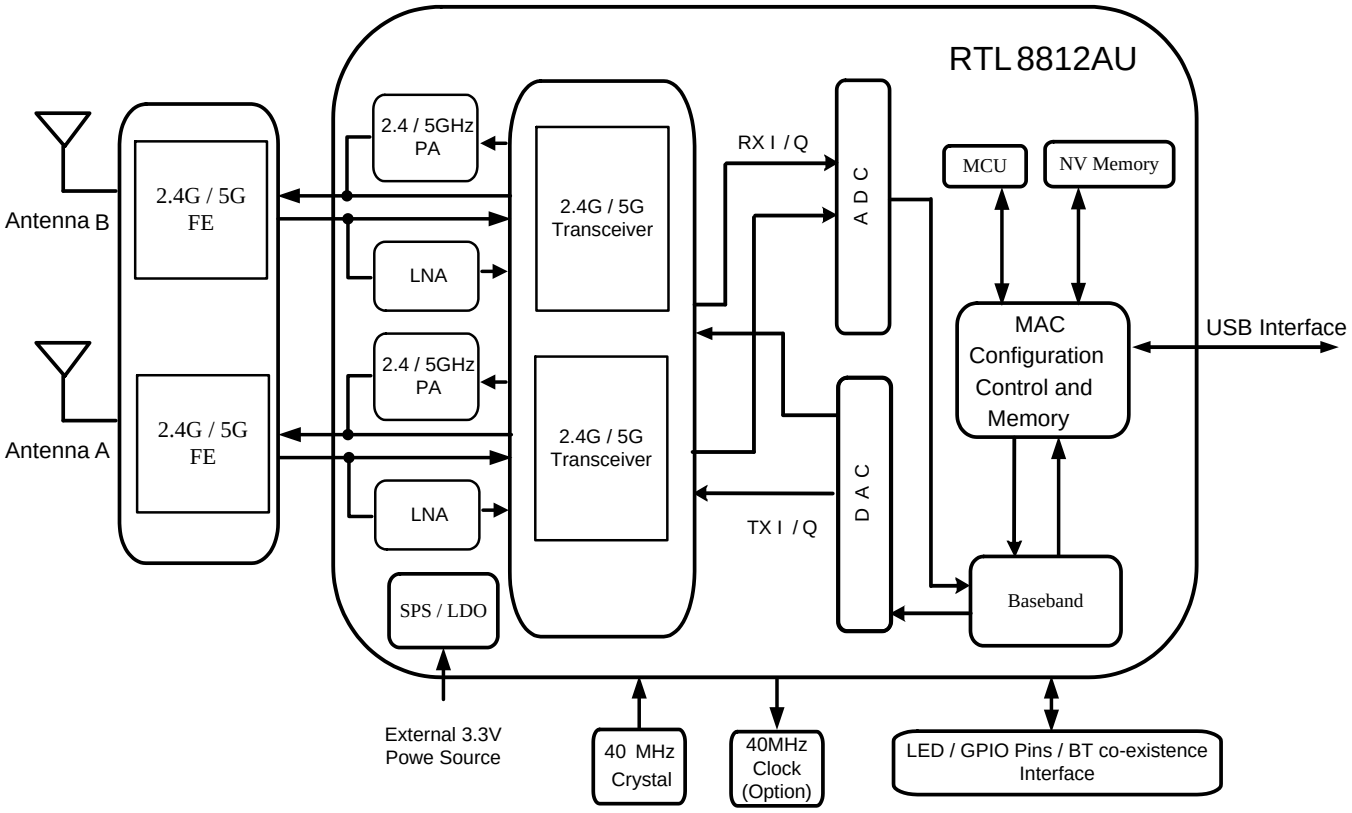


Figure 1. Dual-Band MIMO 2x2 Solution－RTL8812AU-CG (11ac 2x2 MAC/BB/RF + PA)

4. Pin Assignments

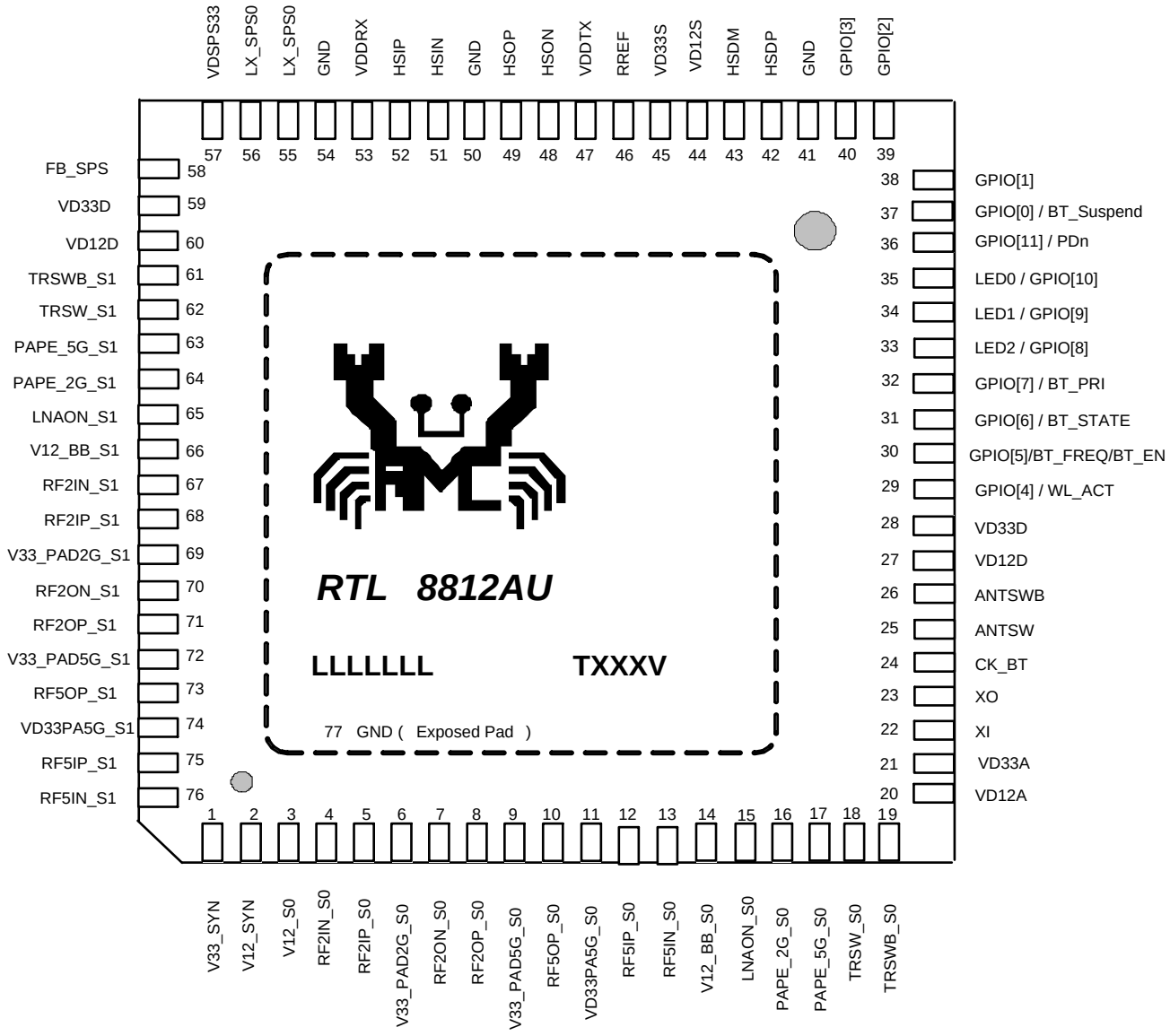


Figure 2. Pin Assignments

4.1. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2.

5. Pin Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin

5.1. USB Express Transceiver Interface

Table 1. USB Transceiver Interface

Symbol	Type	Pin No	Description
HSDP/HSDM	I/O	41, 42	High speed USB Differential Pair
HSON/USOP	O	48, 49	Super speed USB tx differential pair
HSIN/HSIP	I	51, 52	Super speed USB rx differential pair.

5.2. Power Pins

Table 2. Power Pins

Symbol	Type	Pin No	Description
V33_SYN	P	1	3.3V for analog circuits
V12_SYN	P	2	1.2V for analog circuits
V12_S0	P	3	1.2V for analog circuits
V33_PAD2G_S0	P	6	3.3V for analog circuits
V33_PAD5G_S0	P	9	3.3V for analog circuits
VD33PA5G_S0	P	11	3.3V for analog circuits
V12_BB_S0	P	14	1.2V for analog circuits
VD12A	P	20	1.2V for analog circuits
VD33A	P	21	3.3V for analog circuits
VD12S	P	44	1.2V for analog circuits
VD33S	P	45	3.3V for analog circuits
RREF	P	46	Reference current source Connect 6.2k ohm(1%) precision resistor to ground.
VDDTX	P	47	1.2V for analog circuits
VDDRX	P	53	1.2V for analog circuits
LX	P	56, 55	Switching Regulator Output
VDSPS33	P	57	3.3V for analog circuits
FB_SPS	P	58	Switching regulator feedback path. connect with LX.
VD33D	P	59, 28	VDD3.3V for Digital
VD12D	P	60, 27	Digital 1.2V Regulator Output
V12_BB_S1	P	66	1.2V for analog circuits
V33_PAD2G_S1	P	69	3.3V for analog circuits
V33_PAD5G_S1	P	72	3.3V for analog circuits
VD33PA5G_S1	P	74	3.3V for analog circuits
GND	P	54, 50, 41	Ground

5.3. RF Interface

Table 3. RF Interface

Symbol	Type	Pin No	Description
RF2IN_S0	I	4	RF 2.4G Rx0 negative signal
RF2IP_S0	I	5	RF 2.4G Rx0 positive signal
RF2ON_S0	O	7	RF 2.4G Tx0 negative signal
RF2OP_S0	O	8	RF 2.4G Tx0 positive signal
RF5OP_S0	O	10	RF 5G Tx0 positive signal
RF5IP_S0	I	12	RF 5G Rx0 positive signal
RF5IN_S0	I	13	RF 5G Rx0 negative signal

Symbol	Type	Pin No	Description
LNAON_S0	O	15	External LNA_0 enable
PAPE_2G_S0	O	16	2.4GHz Tx power amplifier 0 enable
PAPE_5G_S0	O	17	5 GHz Tx power amplifier 0 enable
TRSW_S0	O	18	Transmit/Receive Path Select 0
TRSWB_S0	O	19	Transmit/Receive Path Select 0
ANTSW	O	25	Antenna select control signal
ANTSWB	O	26	Antenna select control signal
TRSWB_S1	O	61	Transmit/Receive Path Select 1
TRSW_S1	O	62	Transmit/Receive Path Select 1
PAPE_5G_S1	O	63	5GHz Tx power amplifier 1 enable
PAPE_2G_S1	O	64	2.4 GHz Tx power amplifier 1 enable
LNAON_S1	O	65	External LNA_1 enable
RF2IN_S1	I	67	RF 2.4G Rx1 negative signal
RF2IP_S1	I	68	RF 2.4G Rx1 positive signal
RF2ON_S1	O	70	RF 2.4G Tx1 negative signal
RF2OP_S1	O	71	RF 2.4G Tx1 positive signal
RF5OP_S1	O	73	RF 5G Tx1 positive signal
RF5IP_S1	I	75	RF 5G Rx1 positive signal
RF5IN_S1	I	76	RF 5G Rx1 negative signal

5.4. LED Interface

Table 4. LED Interface

Symbol	Type	Pin No	Description
LED2 / GPIO[8]	O	33	LED pins (Active Low) The pin is also shared with GPIO9 and can be selected by control register
LED1 / GPIO[9]	O	34	LED pins (Active Low) The pin is also shared with GPIO10 and can be selected by control register
LED0 / GPIO[10]	O	35	LED pins (Active Low) The pin is also shared with GPIO8 and can be selected by control register

5.5. Clock and Other Pins

Table 5. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	22	40MHz OSC Input. Input of 40MHz Crystal clock reference
XO	O	23	Output of 40MHz Crystal Clock Reference
CK_BT	O	24	buffered 40MHz clock outputs for other peripheral IC

Symbol	Type	Pin No	Description
GPIO[4] / WL_ACT	IO	29	General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_ACT Pin. The WLAN_ACT signal indicates when WLAN is either transmitting or receiving in the 2.4GHz ISM band.
GPIO[5] / BT_FREQ / BT_EN	IO	30	General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_RX Pin. WLAN_RX is an indicator for wireless LAN RX activity.
GPIO[6] / BT_STATE	IO	31	General Purpose Input/Output Pin or Bluetooth Coexistence BT_STAT Pin. The BTSTAT signal indicates when normal Bluetooth packets are being transmitted or received.
GPIO[7] / BT_PRI	IO	32	General Purpose Input/Output Pin or Bluetooth Coexistence BT_PRI Pin. The BT_PRI signal indicates when a high priority Bluetooth packet is being transmitted or received.
PDn / GPIO[11]	I	36	This Pin can externally shutdown the RTL8812AU (no requirement for an extra power switch) or turn the WLAN radio off through the host interface according to internal the setting of internal non-volatile memory. This pin is also shared with GPIO11.
GPIO[0] / BT_Suspend	IO	37	General Purpose Input/Output Pin or Bluetooth enable/disable inform input pin.
GPIO[1]	IO	38	General Purpose Input/Output Pin
GPIO[2]	IO	39	General Purpose Input/Output Pin
GPIO[3]	IO	40	General Purpose Input/Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 6. Temperature Limit Ratings

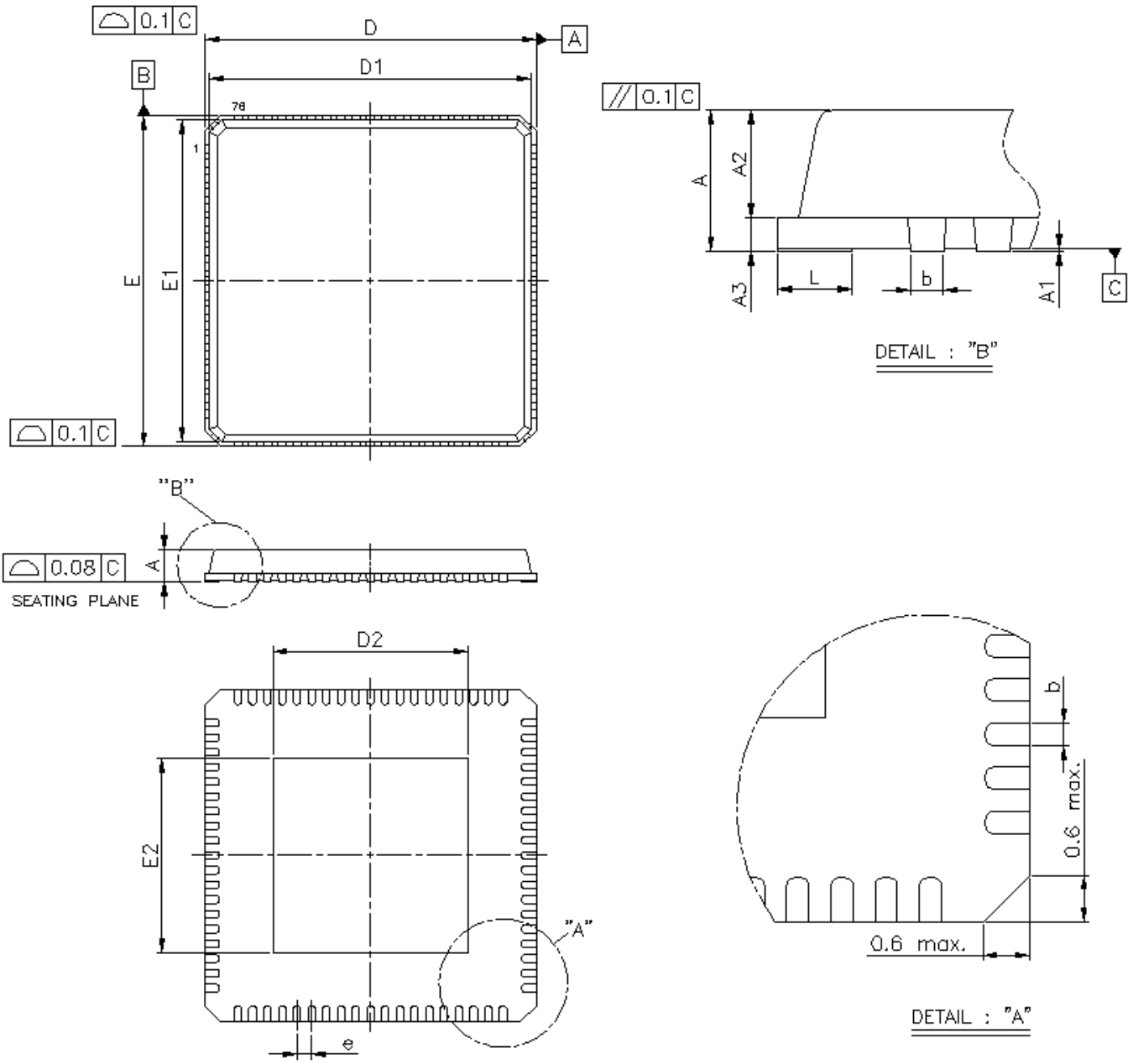
Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

Table 7. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
DVDD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
DVDD12	1.2V Core Supply Voltage	1.10	1.2	1.32	V

7. Mechanical Dimensions



7.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.55	0.65	0.80	0.022	0.026	0.032
A_3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		9.00BSC			0.354BSC	
D_1/E_1		8.75BSC			0.344BSC	
D_2	5.56	5.81	6.06	0.219	0.229	0.239
E_2	6.06	6.31	6.56	0.239	0.249	0.259
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

8. Ordering Information

Table 8. Ordering Information

Part Number	Package	Status
RTL8812AU-CG	QFN-76, 'Green' Package	Engineering sample

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