



**Ameba-Z**

**SINGLE-CHIP 802.11b/g/n 1T1R WLAN SoC**

**DATASHEET**

**(CONFIDENTIAL: Development Partners Only)**

**2018/05/10**

**Track ID: JATR**



Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

[www.realtek.com](http://www.realtek.com)

**COPYRIGHT**

©2011 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

**DISCLAIMER**

Please Read Carefully:

Realtek Semiconductor Corp., (Realtek) reserves the right to make corrections, enhancements, improvements and other changes to its products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

Reproduction of significant portions in Realtek data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Realtek is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions.

Buyers and others who are developing systems that incorporate Realtek products (collectively, "Customers") understand and agree that Customers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Customers have

full and exclusive responsibility to assure the safety of Customers' applications and compliance of their applications (and of all Realtek products used in or for Customers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Customer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Customer agrees that prior to using or distributing any applications that include Realtek products, Customer will thoroughly test such applications and the functionality of such Realtek products as used in such applications.

Realtek's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation kits, (collectively, "Resources") are intended to assist designers who are developing applications that incorporate Realtek products; by downloading, accessing or using Realtek's Resources in any way, Customer (individually or, if Customer is acting on behalf of a company, Customer's company) agrees to use any particular Realtek Resources solely for this purpose and subject to the terms of this Notice.

Realtek's provision of Realtek Resources does not expand or otherwise alter Realtek's applicable published warranties or warranty disclaimers for Realtek's products, and no additional obligations or liabilities arise from Realtek providing such Realtek Resources. Realtek reserves the right to make corrections, enhancements, improvements and other changes to its Realtek Resources. Realtek has not conducted any testing other than that specifically described in the published documentation for a particular Realtek Resource.

Customer is authorized to use, copy and modify any individual Realtek Resource only in connection with the development of applications that include the Realtek product(s) identified in such Realtek Resource. No other license, express or implied, by estoppel or otherwise to any other Realtek intellectual property right, and no license to any technology or intellectual property right of Realtek or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Realtek products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of Realtek Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from Realtek under the patents or other Realtek's intellectual property.

Realtek's Resources are provided "as is" and with all faults. Realtek disclaims all other warranties or representations, express or implied, regarding resources or use thereof, including but not limited to accuracy or completeness, title, any epidemic failure warranty and any implied warranties of merchantability, fitness for a particular purpose, and non-infringement of any third party intellectual property rights.

Realtek shall not be liable for and shall not defend or indemnify Customer against any claim, including but not limited to any infringement claim that related to or is based on any combination of products even if described in Realtek Resources or otherwise. In no event shall Realtek be liable for any actual, direct, special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of Realtek's Resources or use thereof, and regardless of whether Realtek has been advised of the possibility of such damages. Realtek is not responsible for any failure to meet such industry standard requirements.

Where Realtek specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Customers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any Realtek products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death. Such equipment includes, without limitation, all medical devices identified by the U.S.FDA as Class III devices and equivalent classifications outside the U.S.

Customers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Customers' own risk. Customers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Customer will fully indemnify Realtek and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

#### **TRADEMARKS**

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

#### **USING THIS DOCUMENT**

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

#### **REVISION HISTORY**

<b>Revision</b>	<b>Release Date</b>	<b>Summary</b>
1.0	2016/09/01	Change chapter organization Change features Add timer & RTC datasheet Add all peripherals features Update table list Update package and pin description
1.1	2016/09/01	Add exception table
1.2	2016/09/02	Add package, pin number and dimension information

Revision	Release Date	Summary
1.3	2016/10/21	Fix some errors
1.4	2016/11/03	Advanced time just have 2 groups
1.5	2016/11/29	Fix some errors
1.6	2016/12/09	Add ADC pin definitions
1.7	2016/12/15	Add RTL8710BN-LO Specification
1.8	2016/12/22	Add 3.3V ADC channel for 8710BN(QFN32)
1.9	2016/12/28	Change SPS_LDO_SEL description
2.0	2017/02/13	Change 8711BG to 8711BU (QFN68 with USB) Add backup register spec.
2.1	2017/02/27	Add ordering information
2.2	2017/03/27	Remove 8711BN
2.3	2017/04/10	Change ADC Features in chapter 18.
3.0	2017/09/29	Add 8710BX & 8710BL.
3.3	2018/05/10	Add 8711BN.
3.4	2018/06/05	Change DISCLAIMER

# Table of Contents

<b>1. PRODUCT OVERVIEW .....</b>	<b>12</b>
1.1. GENERAL DESCRIPTION.....	12
1.2. ORDERING INFORMATION .....	12
1.3. FEATURES.....	13
1.4. PERIPHERALS .....	14
1.5. PACKAGE TYPES AND PIN DESCRIPTIONS .....	15
1.5.1. <i>RTL8710BN-A0 (QFN32)</i> .....	15
1.5.2. <i>RTL8710BX-A0 (QFN32)</i> .....	16
1.5.3. <i>RTL8710BL-A0 (QFN32)</i> .....	17
1.5.4. <i>RTL8711BU-A0 (QFN68)</i> .....	18
1.5.5. <i>RTL8711BN-A0 (QFN48)</i> .....	19
1.6. PIN DESCRIPTIONS .....	20
1.6.1. <i>Power On Trap Pin</i> .....	20
1.6.2. <i>RF pin</i> .....	21
1.6.3. <i>CHIP EN</i> .....	21
1.6.4. <i>Power Pins</i> .....	21
1.6.5. <i>XTAL Pins</i> .....	22
1.6.6. <i>ADC Pins</i> .....	22
1.6.7. <i>USB Pins</i> .....	22
1.6.8. <i>GPIO Pins</i> .....	23
<b>2. BLOCK DIAGRAM .....</b>	<b>27</b>
2.1. FUNCTIONAL BLOCK DIAGRAM .....	27
2.2. WIFI APPLICATION DIAGRAM .....	28
2.3. POWER SUPPLY APPLICATION DIAGRAM.....	29
<b>3. MEMORY ORGANIZATION .....</b>	<b>30</b>
3.1. INTRODUCTION .....	30
3.2. MEMORY MAP AND REGISTER BOUNDARY ADDRESSES .....	30
3.3. INTERNAL ROM.....	31
3.4. INTERNAL SRAM .....	31
3.5. EXTERNAL SPI NOR FLASH .....	31
3.5.1. <i>Features</i> .....	31

3.5.2.	<i>Supported NOR Flash List</i> .....	32
3.5.3.	<i>Electrical Specifications</i> .....	33
<b>4.</b>	<b>EXCEPTION TABLE</b> .....	<b>34</b>
<b>5.</b>	<b>PINMUX ALTERNATE FUNCTIONS</b> .....	<b>36</b>
<b>6.</b>	<b>PMU</b> .....	<b>38</b>
6.1.	FEATURES.....	38
6.2.	POWER MODE AND POWER CONSUMPTION.....	38
6.3.	SHUTDOWN MODE.....	38
6.4.	DEEP SLEEP MODE.....	39
6.4.1.	<i>Power Domain</i> .....	39
6.4.2.	<i>Wakeup Source</i> .....	40
6.5.	DEEP STANDBY MODE.....	40
6.5.1.	<i>Power Domain</i> .....	40
6.5.2.	<i>Wakeup Source</i> .....	41
6.6.	SLEEP POWER GATE.....	41
6.6.1.	<i>Power Domain</i> .....	41
6.6.2.	<i>Wakeup source</i> .....	41
6.7.	SLEEP CLOCK GATE.....	42
6.7.1.	<i>Power Domain</i> .....	42
6.7.2.	<i>Wakeup source</i> .....	42
<b>7.</b>	<b>FIRMWARE PROTECTION</b> .....	<b>44</b>
7.1.	TRUST-ZONE LITE.....	44
<b>8.</b>	<b>WIFI</b> .....	<b>45</b>
8.1.	GENERAL.....	45
8.2.	STANDARDS SUPPORTED.....	45
8.3.	WLAN MAC FEATURES.....	45
8.4.	WLAN PHY FEATURES.....	46
<b>9.</b>	<b>BASIC TIMER</b> .....	<b>47</b>
9.1.	INTRODUCTION.....	47
9.2.	FEATURES.....	47
<b>10.</b>	<b>CAPTURE TIMER</b> .....	<b>48</b>
10.1.	INTRODUCTION.....	48
10.2.	FEATURES.....	48

<b>11.</b>	<b>PWM TIMER .....</b>	<b>49</b>
11.1.	INTRODUCTION .....	49
11.2.	FEATURES.....	49
11.3.	FUNCTION DESCRIPTION.....	49
11.3.1.	<i>PWM mode</i> .....	49
<b>12.</b>	<b>RTC .....</b>	<b>51</b>
12.1.	INTRODUCTION .....	51
12.2.	FEATURES.....	51
12.3.	CLOCK AND PRESCALERS .....	51
12.4.	RTC RESET.....	52
<b>13.</b>	<b>BACKUP REGISTER.....</b>	<b>53</b>
13.1.	INTRODUCTION .....	53
13.2.	BACKUP REGISTER API .....	53
13.3.	BACKUP REGISTER RESET .....	53
<b>14.</b>	<b>UART.....</b>	<b>54</b>
14.1.	INTRODUCTION .....	54
14.2.	FEATURES.....	54
14.3.	BAUD RATE .....	54
14.4.	UART INTERFACE SIGNAL LEVELS .....	55
<b>15.</b>	<b>SPI .....</b>	<b>56</b>
15.1.	INTRODUCTION .....	56
15.2.	FEATURES.....	57
<b>16.</b>	<b>I2C.....</b>	<b>58</b>
16.1.	INTRODUCTION .....	58
16.2.	FEATURES.....	59
<b>17.</b>	<b>I2S .....</b>	<b>60</b>
17.1.	INTRODUCTION .....	60
17.2.	FEATURES.....	60
17.3.	FUNCTION DESCRIPTION.....	60
17.3.1.	<i>Clock Type</i> .....	60
<b>18.</b>	<b>ADC.....</b>	<b>61</b>
18.1.	INTRODUCTION .....	61
18.2.	FEATURES.....	61

18.3.	CHANNEL DESCRIPTION .....	61
<b>19.</b>	<b>GDMA .....</b>	<b>62</b>
19.1.	INTRODUCTION .....	62
19.2.	FEATURES OF GDMA .....	62
<b>20.</b>	<b>WGT (WATCHDOG TIMER).....</b>	<b>63</b>
20.1.	INTRODUCTION .....	63
20.2.	FEATURES.....	63
<b>21.</b>	<b>GPIO .....</b>	<b>64</b>
21.1.	INTRODUCTION .....	64
21.2.	FEATURES OF GPIO .....	64
<b>22.</b>	<b>SECURITY ENGINE .....</b>	<b>65</b>
22.1.	INTRODUCTION .....	65
22.2.	FEATURES.....	65
<b>23.</b>	<b>USOC (USB DEVICE).....</b>	<b>66</b>
23.1.	INTRODUCTION .....	66
23.2.	FEATURES.....	66
<b>24.</b>	<b>SDIO/GSPI DEVICE.....</b>	<b>67</b>
24.1.	INTRODUCTION .....	67
24.2.	FEATURES.....	67
24.3.	BUS TIMING SPECIFICATION .....	67
<b>25.</b>	<b>ELECTRICAL CHARACTERISTICS .....</b>	<b>70</b>
25.1.	TEMPERATURE LIMIT RATINGS.....	70
25.2.	POWER SUPPLY DC CHARACTERISTICS .....	70
25.3.	DIGITAL IO PIN DC CHARACTERISTICS .....	70
25.3.1.	<i>Electrical Specifications.....</i>	70
<b>26.</b>	<b>MECHANICAL DIMENSIONS.....</b>	<b>72</b>
26.1.	PACKAGE SPECIFICATION .....	72
26.1.1.	<i>QFN32 .....</i>	72
26.1.2.	<i>QFN48 .....</i>	74
26.1.3.	<i>QFN68 .....</i>	76



## List of Tables

TABLE 1-1 AMEBA-Z FEATURES .....	13
TABLE 1-2 AMEBA-Z PERIPHERALS .....	14
TABLE 1-3 PIN DESCRIPTION .....	20
TABLE 1-4 POWER ON TRAP PINS .....	20
TABLE 1-5 RF PIN .....	21
TABLE 1-6 CHIP EN .....	21
TABLE 1-7 POWER PINS .....	21
TABLE 1-8 XTAL PINS .....	22
TABLE 1-9 ADC PINS .....	22
TABLE 1-10 USB PINS .....	22
TABLE 1-11 AMEBA-Z GPIO .....	23
TABLE 3-1 AMEBA-Z MEMORY MAP .....	30
TABLE 3-2 FLASH SUPPORTED .....	32
TABLE 3-3 FLASH BUS DC PARAMETERS .....	33
TABLE 4-1 EXCEPTION TABLE .....	34
TABLE 5-1 PINMUX ALTERNATE FUNCTION MAPPING .....	36
TABLE 6-1 POWER MODE BRIEF SUMMARY AND TYPICAL POWER CONSUMPTION AND RESUME TIME .....	38
TABLE 6-2 DEEP SLEEP MODE POWER DOMAIN .....	39
TABLE 6-3 DEEP SLEEP WAKEUP SOURCE .....	40
TABLE 6-4 DEEP STANDBY POWER DOMAIN .....	40
TABLE 6-5 DEEP STANDBY WAKEUP SOURCE .....	41
TABLE 6-6 SLEEP POWER GATE WAKEUP SOURCE .....	41
TABLE 6-7 SLEEP CLOCK GATE WAKEUP SOURCE .....	42
TABLE 9-1 BASIC TIMER FEATURES .....	47
TABLE 10-1 CAPTURE TIMER FEATURES .....	48
TABLE 11-1 PWM TIMER FEATURES .....	49
TABLE 14-1 UART BAUD RATE .....	54
TABLE 24-1 SDIO INTERFACE TIMING PARAMETERS .....	67
TABLE 25-1 TEMPERATURE LIMIT RATINGS .....	70
TABLE 25-2 POWER SUPPLY DC CHARACTERISTICS .....	70
TABLE 25-3 TYPICAL DIGITAL IO DC PARAMETERS (3.3V CASE) .....	70

---

TABLE 25-4 TYPICAL DIGITAL IO DC PARAMETERS (1.8V CASE) .....	71
TABLE 26-1 QFN32 PACKAGE SPECIFICATION .....	72
TABLE 2 QFN48 PACKAGE SPECIFICATION .....	74
TABLE 26-3 QFN68 PACKAGE SPECIFICATION .....	76

---

---

## List of Figures

---

FIGURE 1 RTL8710BN-A0 QFN32 PIN ASSIGNMENTS .....	15
FIGURE 2 RTL8710BX-A0 QFN32 PIN ASSIGNMENTS .....	16
FIGURE 3 RTL8710BL-A0 QFN32 PIN ASSIGNMENTS .....	17
FIGURE 4 RTL8711BU-A0 QFN68 PIN ASSIGNMENTS .....	18
FIGURE 5 RTL8711BN QFN48 PIN ASSIGNMENTS .....	19
FIGURE 6 BLOCK DIAGRAM.....	27
FIGURE 7 SINGLE-BAND 11N (1X1) SOLUTION.....	28
FIGURE 8 POWER SUPPLY ARCHITECTURE .....	29
FIGURE 9 SHUTDOWN MODE .....	38
FIGURE 10 DEEP SLEEP MODE.....	39
FIGURE 11 DEEP STANDBY MODE .....	40
FIGURE 12 SPI SERIAL FORMAT (SCPH = 0) .....	56
FIGURE 13 SPI SERIAL FORMAT (SCPH = 1) .....	56
FIGURE 14 SLAVE SELECTION.....	57
FIGURE 15 I2C START STOP CONDITION.....	58
FIGURE 16 MASTER/SLAVE AND TRANSMITTER/RECEIVER RELATIONSHIPS.....	58
FIGURE 17 7-BIT ADDRESS FORMAT .....	59
FIGURE 18 10-BIT ADDRESS FORMAT .....	59
FIGURE 19 SDIO BUS TIMING .....	67
FIGURE 20 QFN32 PACKAGE SPECIFICATION.....	72
FIGURE 21 QFN48 PACKAGE SPECIFICATION.....	74
FIGURE 22 QFN68 PACKAGE SPECIFICATION.....	76

---

# 1. Product Overview

## 1.1. General Description

Ameba-Z is a highly integrated single-chip low power 802.11n Wireless LAN (WLAN) network controller. It combines an ARM-CM4 MCU, WLAN MAC, a 1T1R capable WLAN baseband, and RF in a single chip. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different applications and control usage.

Ameba-Z integrates internal memories for complete WIFI protocol functions. The embedded memory configuration also provides simple application developments.

## 1.2. Ordering Information

<i>Part Number</i>	<i>Package</i>	<i>Status</i>
<i>RTL8710BN-A0-CG</i>	QFN32	MP
<i>RTL8711BU-A0-CG</i>	QFN68	MP
<i>RTL8710BL-A0-CG</i>	QFN32	MP@Q4
<i>RTL8710BX-A0-CG</i>	QFN32	MP@Q4
<i>RTL8710BX-VT1-CG</i>	QFN32	ES
<i>RTL8711BN-A0</i>	QFN48	ES

### 1.3. Features

**Table 1-1 Ameba-Z Features**

<b>Feature list</b>		<b>RTL8711BU-A0</b>	<b>RTL8710BN-A0</b>	<b>RTL8710BL-A0</b>	<b>RTL8710BX-A0</b>	<b>RTL8711BN-A0</b>
<b>Package</b>	trays and tape-in-reel	(8x8mm <sup>2</sup> ) QFN68	(5x5mm <sup>2</sup> ) QFN32	(5x5mm <sup>2</sup> ) QFN32	(5x5mm <sup>2</sup> ) QFN32	(6x6mm <sup>2</sup> ) QFN48
<b>Integrated core</b>	Core type	ARM CM4F	ARM CM4F	ARM CM4F	ARM CM4F	ARM CM4F
	Core clock maximum freq.	125MHz	125MHz	125MHz	62.5MHz	125MHz
	Internal SRAM	256KB	256KB	256KB	256KB	256KB
	External FLASH	128M Bytes 4IO	128M Bytes 4IO	128M Bytes 2IO	128M Bytes 2IO	128M Bytes 4IO
<b>FPU</b>	Float process unit	Yes	Yes	Yes	Yes	Yes
<b>SWD/JTAG</b>		SWD	SWD	SWD	SWD	SWD
<b>Backup register</b>	Backup register for power save	16B	16B	16B	16B	16B
<b>Boot Reason</b>	SystemReset/WDG/BOR	Yes	Yes	Yes	Yes	Yes
<b>Security</b>	① SSL/TLS	①	①	①	①	①
	② flash Encryption	②	②	③		②
	③ Trust-Zone Lite (4KB)	③	③			③
<b>WIFI</b>	802.11 B/G/N	Yes	Yes	Yes	Yes	Yes
<b>HT40</b>		Yes	Yes	Yes	NO	Yes
<b>BOR</b>	BOR Detection	Yes	Yes	Yes	Yes	Yes
<b>GPIO</b>	IN/OUT/INT	39	17	10	17	26
<b>Ext. 32K</b>	External 32K	1	1	0	0	1
<b>Dsleep Wakepin</b>	Deep sleep wake pin	4	4	2	4	4

## 1.4. Peripherals

**Table 1-2 Ameba-Z Peripherals**

Feature list			RTL8711BU-A0	RTL8710BN-A0	RTL8710BL-A0	RTL8710BX-A0	RTL8711BN-A0
<i>peripherals</i>	UART	Normal-UART	2	1	1	1	2
		Log-UART	1	1	1	1	1
	SPI Master	Max. 31.25Mbps	1	1	0	1	1
		Max. 31.25Mbps	1	1	0	1	1
	I2C	Max. 400Kbps	2	2	2	2	2
	ADC	VBAT	0~5V	0~5V	NA	NA	NA
		Normal	0~3.3V (X2)	0~3.3V (X1)	NA	0~3.3V (X1)	0~3.3V (X2)
	GDMA	2*6 channels	2	2	2	2	2
	I2S		1	0	0	0	1
	RTC	D/H/M/S	1	1	1	1	1
		OUTPUT	1	1	1	1	1
	Timer	Basic (32K)	4	4	4	4	4
		Advanced (XTAL)	2	2	2	2	2
	PWM	OUTPUT	6	6	4	6	6
		INPUT Capture	2	2	1	2	2
	WDG	Watch Dog	1	1	1	1	1
	USB device		1	0	0	0	0
SDIO 2.0 Device		1	1	0	1	1	

## 1.5. Package Types and Pin Descriptions

### 1.5.1. RTL8710BN-A0 (QFN32)

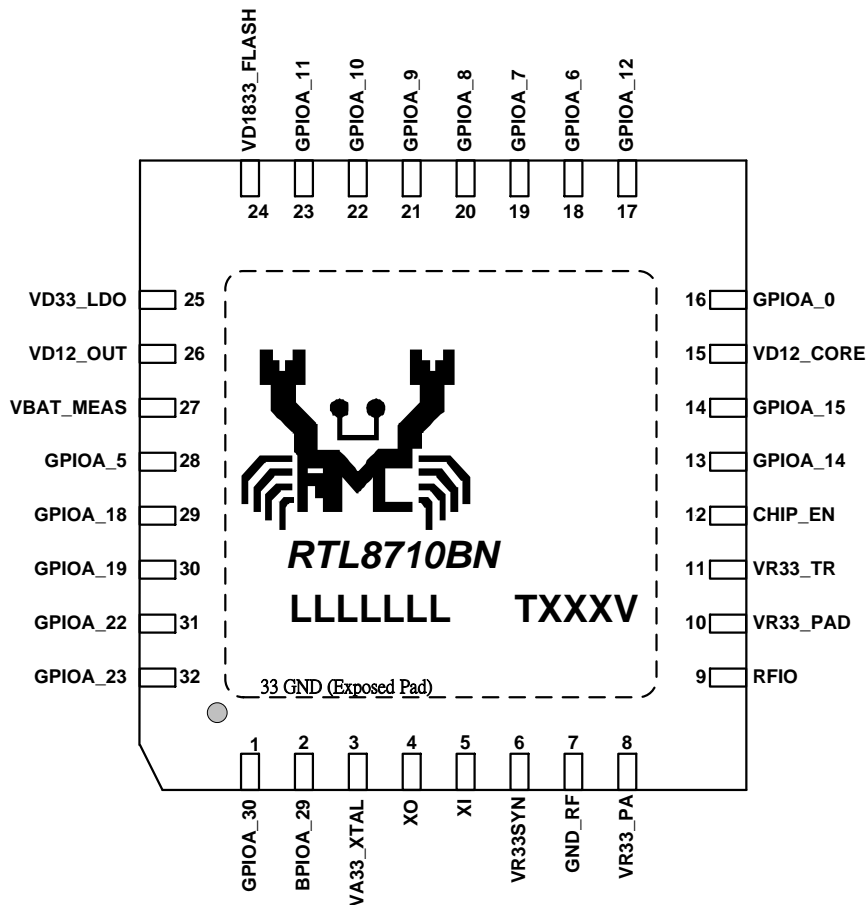


Figure 1 RTL8710BN-A0 QFN32 Pin Assignments

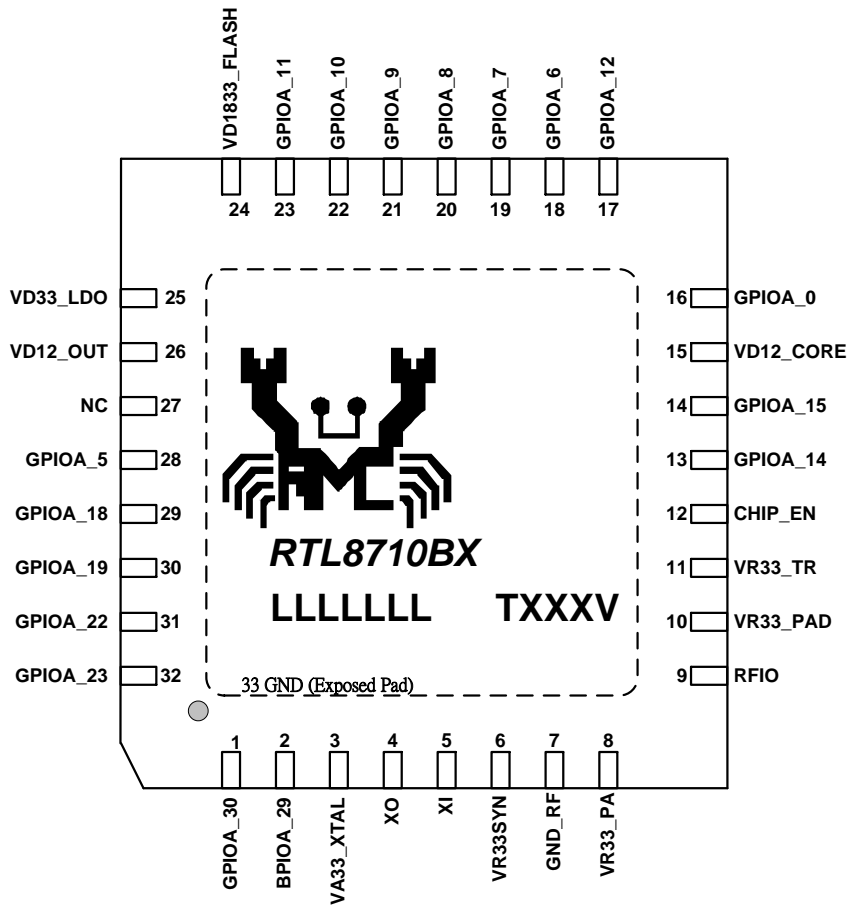
**1.5.2. RTL8710BX-A0 (QFN32)**


Figure 2 RTL8710BX-A0 QFN32 Pin Assignments



### 1.5.3. RTL8710BL-A0 (QFN32)

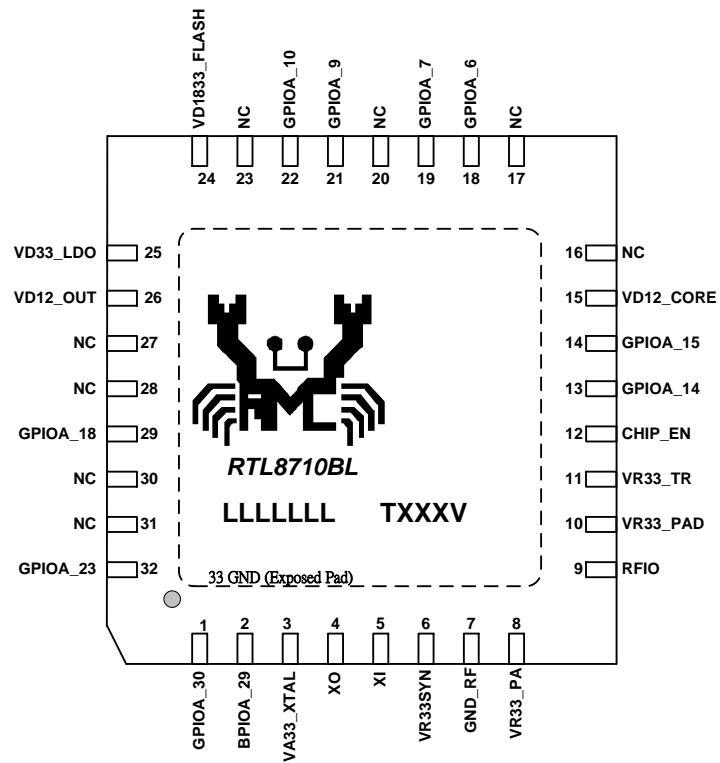


Figure 3 RTL8710BL-A0 QFN32 Pin Assignments

### 1.5.4. RTL8711BU-A0 (QFN68)

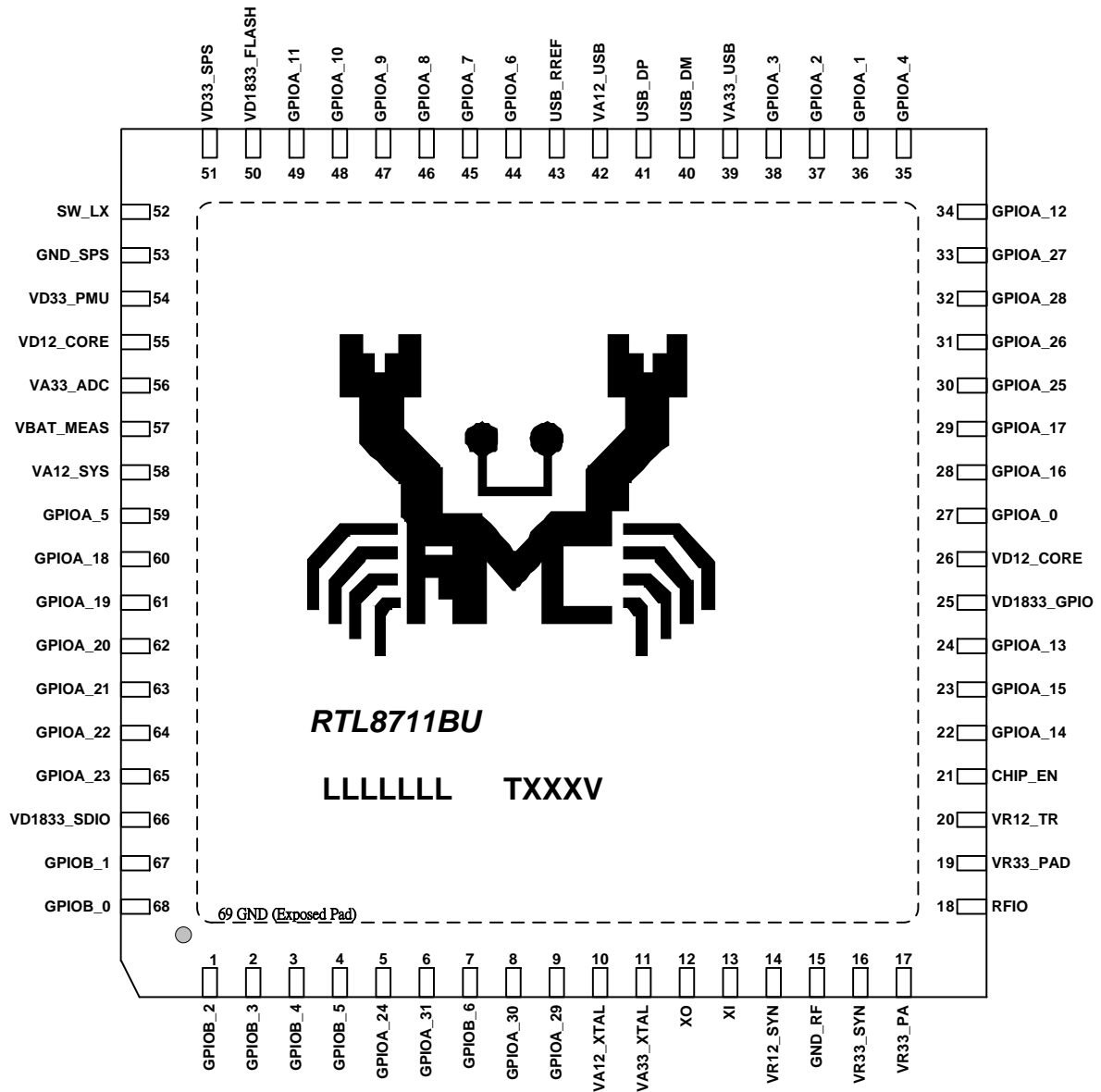


Figure 4 RTL8711BU-A0 QFN68 Pin Assignments

### 1.5.5. RTL8711BN-A0 (QFN48)

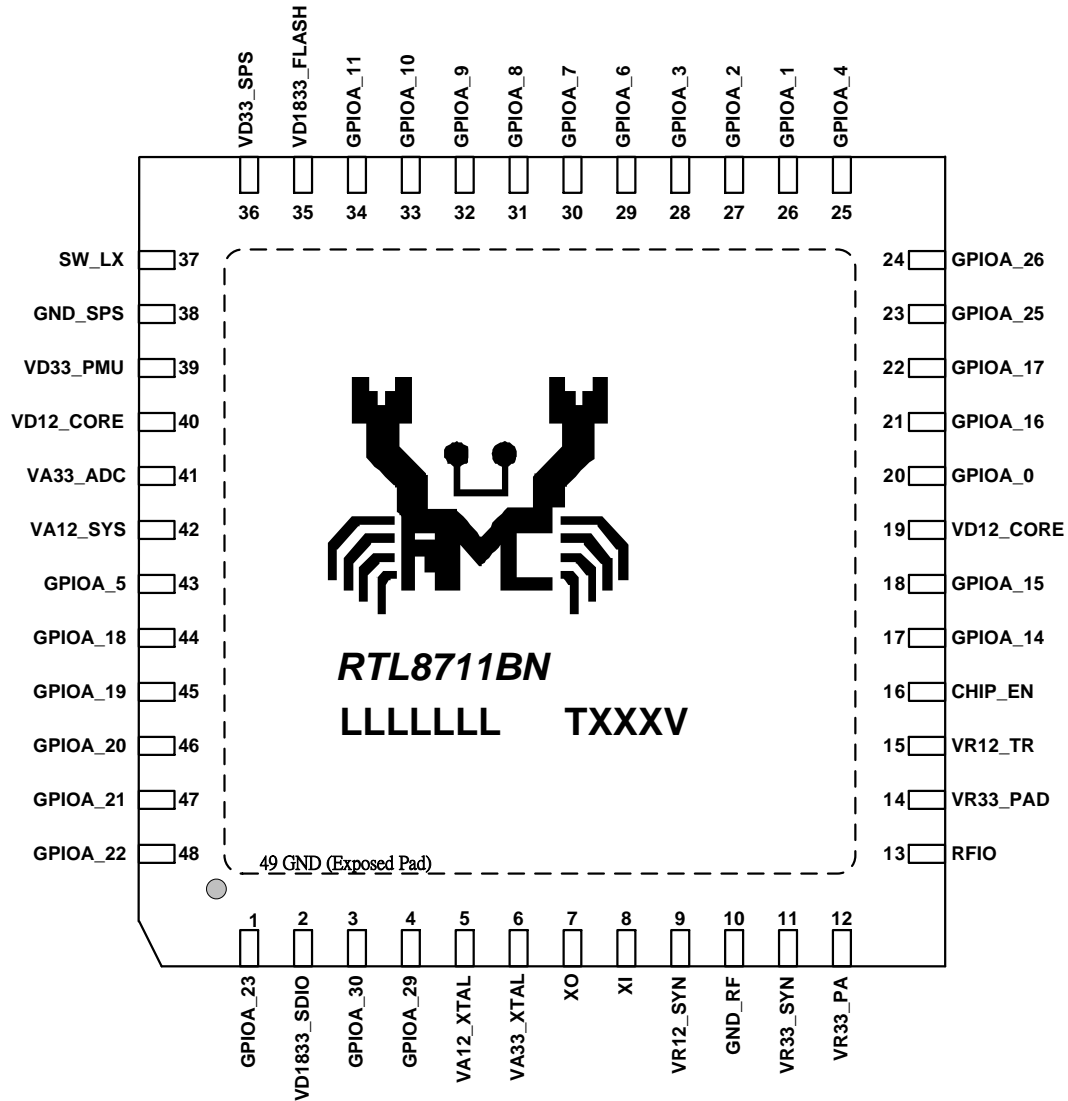


Figure 5 RTL8711BN QFN48 Pin Assignments

## 1.6. Pin Descriptions

The following signal type codes are used in the tables:

**Table 1-3 Pin Description**

<i>I:</i>	<i>Input</i>	<i>O:</i>	<i>Output</i>
<i>T/S:</i>	Tri-State bi-directional input/output pin	<i>S/T/S:</i>	Sustained Tri-State
<i>O/D:</i>	Open Drain	<i>P:</i>	Power pin

### 1.6.1. Power On Trap Pin

**Table 1-4 Power On Trap Pins**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>QFN48</i>	<i>Description</i>
<i>TEST_MODE_SEL</i>	I	27	16	20	Shared with GPIOA_0 1: Enter into test/debug mode 0: Normal operation mode
<i>UART_DOWNLOAD</i>	I	8	1	3	Shared with GPIOA_30 1: Boot from flash 0: Download image from UART
<i>SPS_LDO_SEL</i>	I	38	NA	28	Shared with GPIOA_3 1: LDO 0: SWR

## 1.6.2. RF pin

**Table 1-5 RF pin**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>QFN48</i>	<i>Description</i>
RF_IO	IO	18	9	13	WL RF signal

## 1.6.3. CHIP EN

**Table 1-6 CHIP EN**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>QFN48</i>	<i>Description</i>
CHIP_EN	I	21	12	16	Enable chip. 1: enable chip; 0: shutdown chip

## 1.6.4. Power Pins

**Table 1-7 Power Pins**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>QFN48</i>	<i>Description</i>
VA33_XTAL	P	11	3	6	3.3V for Crystal Oscillator
VA12_XTAL	P	10	NA	5	1.2V for Crystal Oscillator
VR33_SYN	P	16	6	11	3.3V for RF Synthesizer
VR12_SYN	P	14	NA	9	1.2V for RF Synthesizer
VR33_PA	P	17	8	12	3.3V for RF Power amplifier
VR33_PAD	P	19	10	14	3.3V for RF
VR33_TR	P	NA	11	NA	3.3V for RF
VR12_TR	P	20	NA	15	1.2V for RF
VD12_CORE	P	26	15	19	1.2V for digital core power
VD1833_FLASH	P	50	24	35	3.3V/1.8V for Flash IO power
VD33_LDO	P	NA	25	NA	Linear Regulator input from 3.3V to 1.2V
VD33_SPS	P	51	NA	36	Switching/Linear Regulator input from 3.3V to 1.2V
VD12_OUT	P	NA	26	NA	1.2V output from Linear Regulator
SW_LX	P	52	NA	37	1.2V output from Switching/Linear Regulator
GND_SPS	P	53	NA	38	Ground for Switching/Linear Regulator

<b>VA33_USB</b>	P	39	NA	NA	3.3V power for USB Analog
<b>VA12_USB</b>	P	42	NA	NA	1.2V power for USB Analog

### 1.6.5. XTAL Pins

**Table 1-8 XTAL Pins**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>QFN48</i>	<i>Description</i>
<b>XI</b>	I	13	5	8	40MHz OSC Input Input of 40MHz Crystal Clock Reference
<b>XO</b>	O	12	4	7	Output of 40MHz Crystal Clock Reference

### 1.6.6. ADC Pins

**Table 1-9 ADC Pins**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>QFN48</i>	<i>Description</i>
<b>ADC_1</b>	I	61	30	45	ADC input pin, 3.3V tolerance
<b>VBAT_MEAS</b>	I	57	27	NA	ADC input pin, 5V tolerance
<b>ADC_3</b>	I	62	NA	46	ADC input pin, 3.3V tolerance

### 1.6.7. USB Pins

**Table 1-10 USB Pins**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>QFN48</i>	<i>Description</i>
<b>USB_DP</b>	I/O	41	NA	NA	USB differential bus
<b>USB_DM</b>	I/O	40	NA	NA	USB differential bus
<b>USB_RREF</b>	I	43	NA	NA	External reference resistor for USB Analog, 1% accuracy

### 1.6.8. GPIO Pins

**Table 1-11 Ameba-Z GPIO**

<i>Symbol</i>	<i>Type</i>	<i>QFN68</i>	<i>QFN32</i>	<i>RTL8710BL-QFN32</i>	<i>QFN48</i>	<i>Description</i>
GPIOA_14	I/O	22	13	13	17	PWM0
						SWD_CLK
GPIOA_15	I/O	23	14	14	18	PWM1
						SWD_DATA
GPIOA_13	I/O	24	NA	NA	NA	PWM4
GPIOA_0	I/O	27	16	NA	20	PWM2
						EXT_32K
						WL_LED
GPIOA_16	I/O	28	NA	NA	21	UART2_Log_RXD
						PWM1
						RTC_OUT
GPIOA_17	I/O	29	NA	NA	22	UART2_Log_TXD
						PWM2
GPIOA_25	I/O	30	NA	NA	23	UART1_RXD
GPIOA_26	I/O	31	NA	NA	24	UART1_TXD
GPIOA_28	I/O	32	NA	NA	NA	I2C1_SCL
GPIOA_27	I/O	33	NA	NA	NA	I2C1_SDA
GPIOA_12	I/O	34	17	NA	NA	PWM3
GPIOA_4	I/O	35	NA	NA	25	UART0_TXD
						SPI1_MOSI
						SPIO_MOSI
						I2C0_SDA
GPIOA_1	I/O	36	NA	NA	26	UART0_RXD
						SPI1_CLK
						SPIO_SCK
						I2C0_SCL
GPIOA_2	I/O	37	NA	NA	27	UART0_CTS

						SPI1_CS
						SPIO_CS
						I2C1_SDA
<i>GPIOA_3</i>	I/O	38	NA	NA	28	UART0_RTS
						SPI1_MISO SPS_LDO_SEL
						SPIO_MISO
						I2C1_SCL
<i>GPIOA_6</i>	I/O	44	18	18	29	SPIC_CS
						SD_D2
<i>GPIOA_7</i>	I/O	45	19	19	30	SPIC_DATA1
						SD_D3
<i>GPIOA_8</i>	I/O	46	20	NA	31	SPIC_DATA2
						SD_CMD
<i>GPIOA_9</i>	I/O	47	21	21	32	SPIC_DATA0
						SD_CLK
<i>GPIOA_10</i>	I/O	48	22	22	33	SPIC_CLK
						SD_D0
<i>GPIOA_11</i>	I/O	49	23	NA	34	SPIC_DATA3
						SD_D1
<i>GPIOA_5</i>	I/O	59	28	NA	43	SDIO_SIDEHAND_INT
						PWM4
<i>GPIOA_18</i>	I/O	60	29	29	44	UART0_RXD
						SPI1_CLK
						SPIO_SCK
						I2C1_SCL
						SD_D2
						TIMER4_TRIG
						I2S_MCK
<i>GPIOA_19</i>	I/O	61	30	NA	45	UART0_CTS
						SPI1_CS
						SPIO_CS



						I2C0_SDA
						SD_D3
						TIMER5_TRIG
						I2S_SD_TX
<i>GPIOA_20</i>	I/O	62	NA	NA	46	SD_CMD
						I2S_SD_RX
<i>GPIOA_21</i>	I/O	63	NA	NA	47	SD_CLK
						PWM3
						I2S_CLK
<i>GPIOA_22</i>	I/O	64	31	NA	48	UART0_RTS
						SPI1_MISO
						SPIO_MISO
						I2C0_SCL
						SD_D0
						PWM5
						I2S_WS
<i>GPIOA_23</i>	I/O	64	32	32	1	UART0_TXD
						SPI1_MOSI
						SPIO_MOSI
						I2C1_SDA
						SD_D1
						PWM0
<i>GPIOB_1</i>	I/O	67	NA	NA	NA	SPI1_CLK
						SPIO_SCK
<i>GPIOB_0</i>	I/O	68	NA	NA	NA	SPI1_CS
						SPIO_CS
<i>GPIOB_2</i>	I/O	1	NA	NA	NA	SPI1_MISO
						SPIO_MISO
<i>GPIOB_3</i>	I/O	2	NA	NA	NA	SPI1_MOSI
						SPIO_MOSI
<i>GPIOB_4</i>	I/O	3	NA	NA	NA	SWD_CLK

						I2S_MCK
GPIOB_5	I/O	4	NA	NA	NA	SWD_DATA
						I2S_SD_TX
GPIOA_24	I/O	5	NA	NA	NA	I2S_SD_RX
GPIOA_31	I/O	6	NA	NA	NA	I2S_CLK
GPIOB_6	I/O	7	NA	NA	NA	I2S_WS
GPIOA_30	I/O	8	1	1	3	UART2_Log_TXD
						I2C0_SDA
						PWM3
						RTC_OUT
GPIOA_29	I/O	9	2	2	4	UART2_Log_RXD
						I2C0_SCL
						PWM4

## 2. Block Diagram

### 2.1. Functional Block Diagram

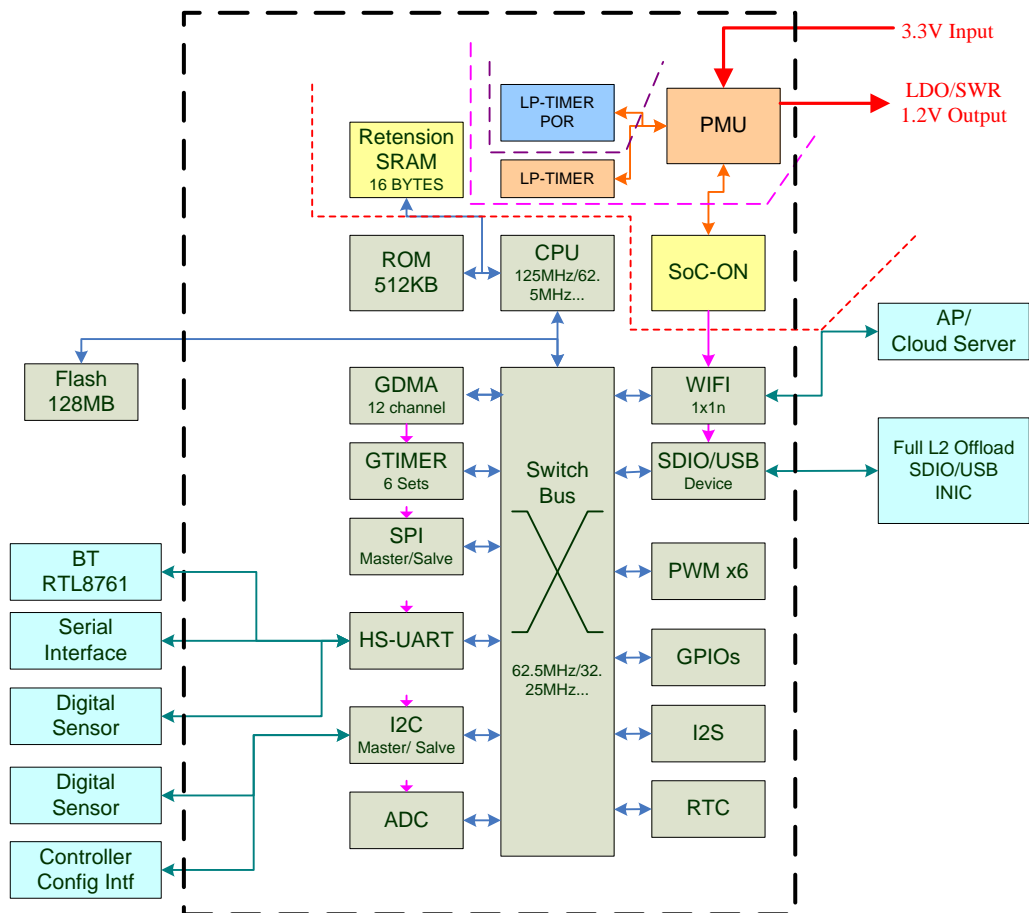


Figure 6 Block Diagram

## 2.2. WIFI Application Diagram

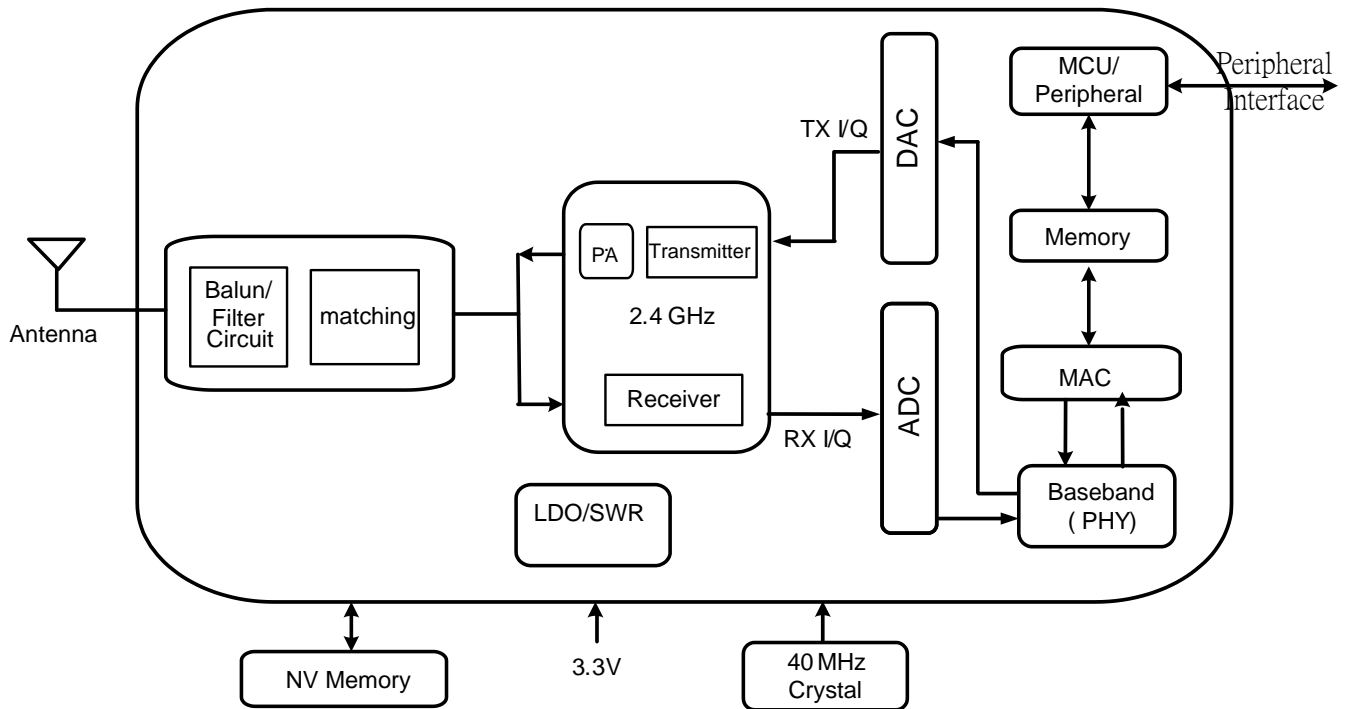
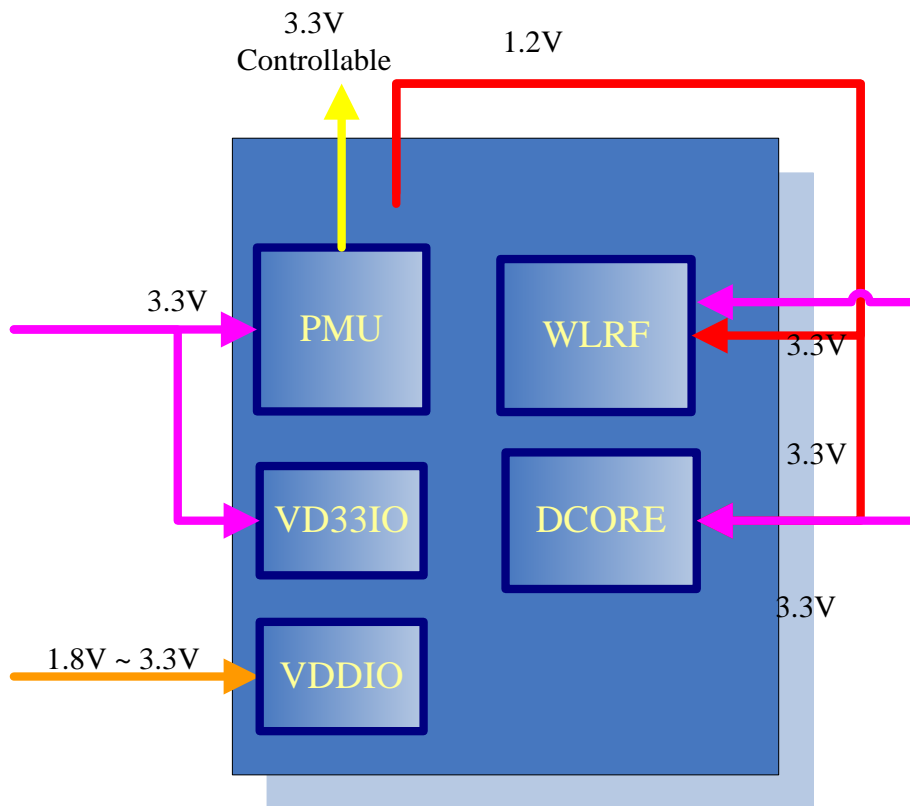


Figure 7 Single-Band 11n (1x1) Solution

## 2.3. Power Supply Application Diagram



**Figure 8 Power Supply Architecture**

The integrated Power Management Unit (PMU) provides the following features:

- 1.2V LDO/SWR(Switching Regulator)
- 3.3V power source integrated power cut controlled by FW.

## 3. Memory organization

### 3.1. Introduction

Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space.

Ameba-Z integrates ROM, internal SRAM, NOR flash controller to provide applications with a variety of memory requirements.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

All the memory areas that are not allocated to on-chip memories and peripherals are considered "Reserved". For the detailed mapping of available memory and register areas, please refer to the Memory map and register boundary addresses chapter and peripheral chapters.

### 3.2. Memory map and register boundary addresses

**Table 3-1 Ameba-Z memory map**

<i>Name</i>	<i>Physical address</i>	<i>size</i>	<i>IP function</i>
<b>ROM</b>	0x0000_0000~0x0007_FFFF	512KB	Internal ROM memory
<b>SRAM</b>	0x1000_0000~0x1001_FFFF	256KB	Internal SRAM memory
<b>FLASH</b>	0x0800_0000~0x0FFF_FFFF	128MB	External Flash memory
<b>SYSON</b>	0x4000_0000~0x4000_0FFF	4KB	SYS Control
<b>GPIO</b>	0x4000_1000~0x4000_17FF	2KB	GPIO Control
<b>Timer</b>	0x4000_2000~0x4000_2FFF	4KB	Timer Control
<b>LOGUART</b>	0x4000_3000~0x4000_33FF	1KB	UART for Log
<b>RTC</b>	0x4000_3400~0x4000_37FF	1KB	RTC control
<b>Cache</b>	0x4000_3C00~0x4000_4FFF	1KB	Flash cache control
<b>ADC</b>	0x4001_0000~0x4001_0FFF	4KB	ADC control
<b>SPIC</b>	0x4002_0000~0x4002_0FFF	4KB	SPI flash controller
<b>UART0</b>	0x4004_0000~0x4004_03FF	1KB	UART0 control
<b>UART1</b>	0x4004_0400~0x4004_07FF	1KB	UART1 control
<b>SPIO</b>	0x4004_2000~0x4004_23FF	1KB	SPIO control
<b>SPI1</b>	0x4004_2400~0x4004_27FF	1KB	SPI1 control
<b>I2C0</b>	0x4004_4000~0x4004_43FF	1KB	I2C0 control
<b>I2C1</b>	0x4004_4400~0x4004_47FF	1KB	I2C1 control
<b>SDIO</b>	0x4005_0000~0x4005_3FFF	16KB	SDIO device control

<b>GDMA0</b>	0x4006_0000~0x4006_07FF	2KB	GDMA0 control
<b>GDMA1</b>	0x4006_1000~0x4006_17FF	2KB	GDMA1 control
<b>I2S</b>	0x4006_2000~0x4006_23FF	1KB	I2S control
<b>IPSEC</b>	0x4007_0000~0x4007_3FFF	16KB	Security control
<b>WIFI</b>	0x4008_0000~0x400B_FFFF	256KB	WIFI register
<b>USB SIE</b>	0x400C_0000~0x400C_0FFF	4KB	USB SIE control
<b>USOC</b>	0x400C_2000~0x400C_2FFF	4KB	USB device register

### 3.3. Internal ROM

512KB ROM is integrated to provide high access speed, low leakage memory. The ROM memory clock speed is up to 125MHz. The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Peripheral Drivers & API
- Non-flash booting functions and drivers
- Security function libs

### 3.4. Internal SRAM

Max. 256KB SRAM is integrated to provide instruction, data, and buffer usage. The maximum clock speed is up to 125MHz.

### 3.5. External SPI NOR Flash

#### 3.5.1. Features

- SPI baud rate:
  - 100/83/71/62/50MHz ...
- Execute in place (XIP):
  - we supports a memory-mapped I/O interface for read operation
  - Support 32K I/D read cache, 2-way associative
  - Support decryption on the fly
- SPI mode:
  - SPI/Dual SPI/DIO SPI/Quad SPI/QIO SPI
- Flash size
  - Support up to 128M Bytes flash size

### 3.5.2. Supported NOR Flash List

**Table 3-2 Flash supported**

<i>Vendor</i>	<i>Part Number</i>	<i>Density</i>	<i>Voltage</i>	<i>IO</i>	<i>Max. Clock</i>
<b>MXIC</b>	MX25L1633E	2MB	3.3V	4I/O	85MHz
<b>MXIC</b>	MX25L3236F	4MB	3.3V	4I/O	104MHz(6 dummy cycle) 133MHz(10 dummy cycle)
<b>MXIC</b>	MX25L6433F	8MB	3.3V	4I/O	80MHz (6 dummy cycle) 133MHz (10 dummy cycle)
<b>MXIC</b>	MX25L12845G	16MB	3.3V	4I/O	70MHz
<b>MXIC</b>	MX25L1606E	2MB	3.3V	2O	80MHz
<b>MXIC</b>	MX25V8006E	1MB	3.3V	2O	70MHz
<b>MXIC</b>	MX25V1635F	2MB	3.3V	4I/O	80MHz
<b>MXIC</b>	MX25V8035F	1MB	3.3V	4I/O	104MHz
<b>MXIC</b>	KH25L8006EM2I-12G	1MB	3.3V	2O	80MHz
<b>MXIC</b>	KH25L1606EM2I-12G	2MB	3.3V	2O	80MHz
<b>MXIC</b>	MX25R1635FM1IH0	2MB	1.8/3.3V	4I/O	80MHz
<b>Winbond</b>	W25Q80DV	1MB	3.3V	4I/O	104MHz
<b>Winbond</b>	W25Q16DV	2MB	3.3V	4I/O	104MHz
<b>Winbond</b>	W25Q32FV	4MB	3.3V	4I/O	104MHz
<b>Winbond</b>	W25R64FV	8MB	3.3V	4I/O	104MHz
<b>Winbond</b>	W25R128FV	16MB	3.3V	4I/O	104MHz
<b>Micron</b>	N25Q032A13ESE40E	4MB	3.3V	4I/O	108MHz
<b>Micron</b>	N25Q064A13ESED0E	8MB	3.3V	4I/O	108MHz
<b>Micron</b>	N25Q128A	16MB	3.3V	4I/O	108MHz
<b>Micron</b>	N25Q00AA13GSF40F	128MB	3.3V	4I/O	108MHz
<b>Gigadevice</b>	GD25Q80C	1MB	3.3V	4I/O	120MHz
<b>Gigadevice</b>	GD25Q16C	2MB	3.3V	4I/O	120MHz
<b>Gigadevice</b>	GD25Q32C	4MB	3.3V	4I/O	120MHz
<b>Gigadevice</b>	GD25Q64C	8MB	3.3V	4I/O	120MHz
<b>Gigadevice</b>	GD25Q128C	16MB	3.3V	4I/O	80MHz



<b>HuaHong</b>	BH25D80A	2MB	3.3V	20	108MHz
<b>ESMT</b>	EN25QH16A	2MB	3.3V	4I/O	104MHz
<b>ESMT</b>	EN25QH16B-104HIP2A	2MB	3.3V	4I/O	104MHz
<b>ESMT</b>	EN25Q80B	1MB	3.3V	4I/O	104MHz
<b>FM</b>	FM25Q08A	2MB	3.3V	4I/O	104MHz

### 3.5.3. Electrical Specifications

Table 3-3 Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
$V_{IH}$	Input-High Voltage	LVTTL	2.0	-	-	V	1
$V_{IL}$	Input-Low Voltage	LVTTL	-	-	0.8	V	2
$V_{OH}$	Output-High Voltage	-	2.4	-	-	V	3
$V_{OL}$	Output-Low Voltage	-	-	-	0.4	V	3
$I_{IL}$	Input-Leakage Current	$V_{IN}=3.3V$ or 0	-10	$\pm 1$	10	$\mu A$	-
$I_{OZ}$	Tri-State Output-Leakage Current	-	-10	$\pm 1$	10	$\mu A$	-
$R_{PU}$	Input Pull-Up Resistance	-	-	75	-	K $\Omega$	4
$R_{PD}$	Input Pull-Down Resistance	-	-	75	-	K $\Omega$	4

**Note 1:**  $V_{IH}$  overshoot:  $V_{IH}(MAX)=V_{DDH} + 2V$  for a pulse width  $\leq 3ns$ .

**Note 2:**  $V_{IL}$  undershoot:  $V_{IL}(MIN)=-2V$  for a pulse width  $\leq 3ns$ .

**Note 3:** The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

**Note 4:** These values are typical values checked in the manufacturing process and are not tested.

## 4. Exception table

**Table 4-1 Exception table**

<b>Exception Number</b>	<b>Exception Type</b>	<b>Description</b>
	Reset	Reset
	NMI	Nonmaskable interrupt (external NMI input). The WDG is linked to the NMI vector
	Hard Fault	All fault conditions if the corresponding fault handler is not enabled
	MemManager Fault	Memory management fault; Memory Protection Unit (MPU) violation or access to illegal locations
	Bus Fault	Bus error; occurs when Advanced High-Performance Bus (AHB) interface receives an error response from a bus slave (also called prefetch abort if it is an instruction fetch or data abort if it is a data access)
	Usage Fault	Exceptions resulting from program error or trying to access coprocessor (the Cortex-M4 does not support a coprocessor)
	RSVD	-
	SVC	Supervisor Call
	Debug Monitor	Debug monitor (breakpoints, watchpoints, or external debug requests)
	RSVD	-
	PendSV	Pendable Service Call
	SYSTICK	System Tick Timer
<b>[0]</b>	System_ISR	
<b>[1]</b>	WDG	Watch dog global interrupt
<b>[2]</b>	Timer0	Timer0 global interrupt
<b>[3]</b>	Timer1	Timer1 global interrupt
<b>[4]</b>	Timer2	Timer2 global interrupt
<b>[5]</b>	Timer3	Timer3 global interrupt
<b>[6]</b>	SPI0	SPI0 global interrupt for communication spi
<b>[7]</b>	GPIO	GPIO portA global interrupt
<b>[8]</b>	UART0	UART0 global interrupt
<b>[9]</b>	SPI_FLASH	SPI Flash global interrupt
<b>[10]</b>	UART1	UART1 global interrupt
<b>[11]</b>	Timer4	Timer4 global interrupt
<b>[12]</b>	SDIO_Dev	SDIO device global interrupt
<b>[13]</b>	I2S0	I2S0 global interrupt
<b>[14]</b>	Timer5	Timer5 global interrupt
<b>[15]</b>	WL_DMA	Wlan Host global interrupt
<b>[16]</b>	WL_PROTOCOL	Wlan Firmware Wlan global interrupt

[17]	CRYPTO	IPsec global interrupt
[18]	SPI1	SPI1 global interrupt for communication spi
[19]	Peripheral_ISR	See Below Table
[20]	GDMA0_Channel0	GDMA0 channel 0 global interrupt
[21]	GDMA0_Channel1	GDMA0 channel 1 global interrupt
[22]	GDMA0_Channel2	GDMA0 channel 2 global interrupt
[23]	GDMA0_Channel3	GDMA0 channel 3 global interrupt
[24]	GDMA0_Channel4	GDMA0 channel 4 global interrupt
[25]	GDMA0_Channel5	GDMA0 channel 5 global interrupt
[26]	I2C0	I2C0 global interrupt
[27]	I2C1	I2C1 global interrupt
[28]	uart log	log uart intr
[29]	adc	adc intr
[30]	rdp_int	cpu rdp protection int
[31]	rtc_int	rtc timer int
[32]	GDMA1_CHANNEL0_IRQ	GDMA1 channel 0 global interrupt
[33]	GDMA1_CHANNEL1_IRQ	GDMA1 channel 1 global interrupt
[34]	GDMA1_CHANNEL2_IRQ	GDMA1 channel 2 global interrupt
[35]	GDMA1_CHANNEL3_IRQ	GDMA1 channel 3 global interrupt
[36]	GDMA1_CHANNEL4_IRQ	GDMA1 channel 4 global interrupt
[37]	GDMA1_CHANNEL5_IRQ	GDMA1 channel 5 global interrupt
[38]	USB_IRQ	USOC interrupt
[39]	RXI300_IRQ	
[40]	USB_SIE	USB SIE interrupt

## 5. Pinmux Alternate Functions

**Table 5-1 Pinmux Alternate Function mapping**

QFN68	QFN32	8710BL QFN32	QFN48	GPIO	UART	SPI Master	SPI Slave	SPI Flash	I2C	SDIO	PWM/TIMER	EXT32K	I2S	Others
✓	✓	✓	✓	PA_14							PWM0	SWD_CLK		
✓	✓	✓	✓	PA_15							PWM1	SWD_DATA		
✓				PA_13							PWM4			
✓	✓		✓	PA_0							PWM2	ext_32K		
✓			✓	PA_16	UART2_log_RXD						PWM1	RTC_OUT		
✓			✓	PA_17	UART2_log_TXD						PWM2			
✓			✓	PA_25	UART1_RXD									
✓			✓	PA_26	UART1_TXD									
✓				PA_28					I2C1_SCL					
✓				PA_27					I2C1_SDA					
✓	✓			PA_12							PWM3			
✓			✓	PA_4	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C0_SDA					
✓			✓	PA_1	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C0_SCL					
✓			✓	PA_2	UART0_CTS	SPI1_CS	SPI0_CS		I2C1_SDA					
✓			✓	PA_3	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C1_SCL					
✓	✓	✓	✓	PA_6				SPIC_CS		SD_D2				
✓	✓	✓	✓	PA_7				SPIC_DATA1		SD_D3				
✓	✓		✓	PA_8				SPIC_DATA2		SD_CMD				
✓	✓	✓	✓	PA_9				SPIC_DATA0		SD_CLK				
✓	✓	✓	✓	PA_10				SPIC_CLK		SD_D0				
✓	✓		✓	PA_11				SPIC_DATA3		SD_D1				
✓	✓		✓	PA_5						SDIO_SIOE_BAND_IN_T	PWM4			WAKEUP_1
✓	✓	✓	✓	PA_18	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C1_SCL	SD_D2	TIMER4_TRIG		I2S_MCK	WAKEUP_0
✓	✓		✓	PA_19	UART0_CTS	SPI1_CS	SPI0_CS		I2C0_SDA	SD_D3	TIMER5_TRIG		I2S_SD_TX	ADC1
✓			✓	PA_20						SD_CMD			I2S_SD_RX	ADC3

✓			✓	PA_21						SD_CLK	PWM3		I2S_CLK	
✓	✓		✓	PA_22	UART0_RTS	SPI1_MIS O	SPI0_MIS O		I2C0_SCL	SD_D0	PWM5		I2S_WS	WAKEUP_ 2
✓	✓	✓	✓	PA_23	UART0_TXD	SPI1_MOS I	SPI0_MOS I		I2C1_SDA	SD_D1	PWM0			WAKEUP_ 3
✓				PB_1		SPI1_CLK	SPI0_SCK							
✓				PB_0		SPI1_CS	SPI0_CS							
✓				PB_2		SPI1_MIS O	SPI0_MIS O							
✓				PB_3		SPI1_MOS I	SPI0_MOS I							
✓				PB_4								SWD_CLK	I2S_MCK	
✓				PB_5								SWD_DAT A	I2S_SD_TX	
✓				PA_24									I2S_SD_RX	
✓				PA_31									I2S_CLK	
✓				PB_6									I2S_WS	
✓	✓	✓	✓	PA_30	UART2_log_T XD				I2C0_SDA		PWM3	RTC_OUT		
✓	✓	✓	✓	PA_29	UART2_log_R XD				I2C0_SCL		PWM4			

## 6. PMU

### 6.1. Features

### 6.2. Power Mode and Power Consumption

Table 6-1 Power Mode Brief Summary and Typical Power Consumption and Resume Time

Power Mode	Power Consumption		
	Typical	Maximum	Units
Deep Sleep Mode	7	7	uA
Deep Standby Mode	70	70	uA
Sleep Power Gate	120	120	uA
Sleep Clock Gate	350	350	uA

### 6.3. Shutdown Mode

- CHIP\_EN deasserts to shutdown whole chip without external power cut components required.

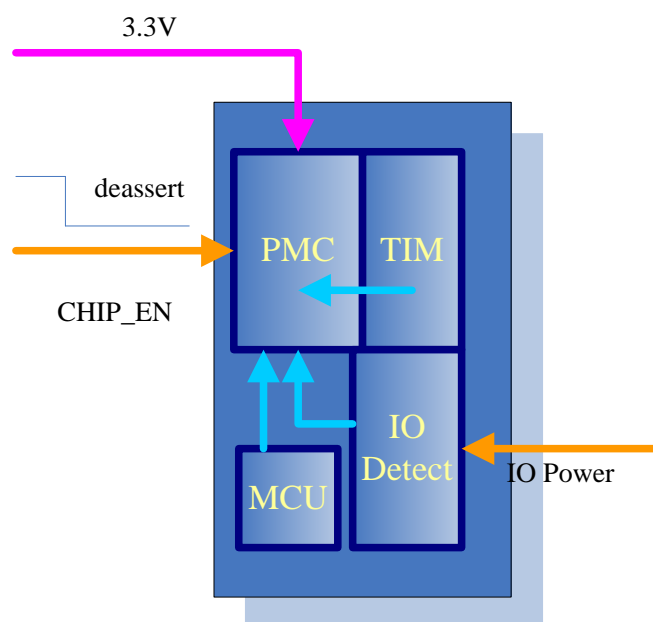


Figure 9 Shutdown Mode

## 6.4. Deep Sleep Mode

- CHIP\_EN keeps high. Enter into Deep Sleep mode by API.

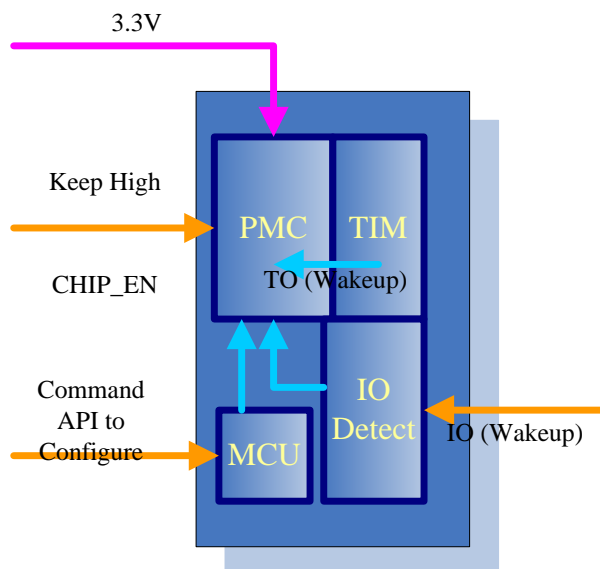


Figure 10 Deep Sleep Mode

### 6.4.1. Power Domain

Table 6-2 Deep Sleep Mode Power Domain

<i>Functions</i>	<i>Power State</i>	<i>Comment</i>
<i>cortex-M4 core</i>	OFF	
<i>system clock</i>	OFF	
<i>SRAM</i>	OFF	
<i>Regulator</i>	OFF	
<i>Peripherals</i>	OFF	
<i>Backup register</i>	OFF	
<i>RTC</i>	OFF	
<i>low precision timer</i>	ON	1
<i>Dsleep wake pin</i>	ON	4

## 6.4.2. Wakeup Source

Table 6-3 Deep Sleep Wakeup Source

Wakeup source	Wakeup	Comment
low precision timer	YES	
Dsleep Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23

## 6.5. Deep Standby Mode

- CHIP\_EN keeps high. Entering into Deep Sleep mode by API.

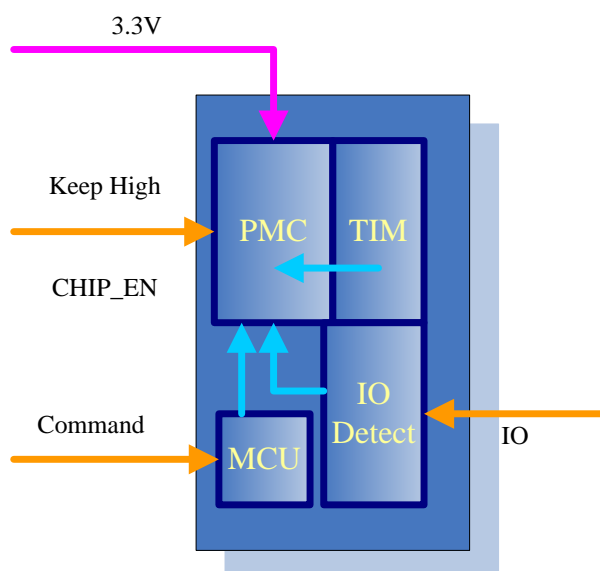


Figure 11 Deep Standby Mode

### 6.5.1. Power Domain

Table 6-4 Deep Standby Power Domain

functions	Power State	comment
cortex-M4 core	OFF	
system clock	OFF	



<i>SRAM</i>	OFF	
<i>Regulator</i>	OFF	
<i>Peripherals</i>	OFF	
<i>Backup register</i>	ON	16B
<i>RTC</i>	ON	
<i>System timer</i>	ON	1
<i>low precision timer</i>	ON	1
wake pin	ON	4

## 6.5.2. Wakeup Source

Table 6-5 Deep Standby Wakeup Source

<i>Wakeup source</i>	<i>Wakeup</i>	<i>Comment</i>
<i>Wake pin</i>	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
<i>RTC</i>	YES	
<i>System timer</i>	YES	
<i>low precision timer</i>	YES	

## 6.6. Sleep Power Gate

### 6.6.1. Power Domain

Sleep mode turn off power domain including cortex-M4 core, and system clock. System is not required to restart after wakeup.

### 6.6.2. Wakeup source

Table 6-6 Sleep Power Gate Wakeup Source

<i>Wakeup source</i>	<i>Wakeup</i>	<i>comment</i>
<i>GPIO interrupt</i>	YES	High/Low active
<i>general purpose timer</i>	YES	

<i>wlan</i>	YES	
<i>ADC</i>	YES	
<i>UART</i>	YES	
<i>I2C</i>	YES	
<i>SDIO/GSPI</i>	YES	
<i>USB</i>	YES	
<i>Wake pin</i>	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
<i>RTC</i>	YES	
<i>System timer</i>	YES	
<i>low precision timer</i>	YES	

## 6.7. Sleep Clock Gate

### 6.7.1. Power Domain

Sleep mode turn off system clock. System is not required to restart after wakeup.

### 6.7.2. Wakeup source

Table 6-7 Sleep Clock Gate Wakeup Source

<i>Wakeup source</i>	<i>Wakeup</i>	<i>comment</i>
<i>GPIO interrupt</i>	YES	High/Low active
<i>general purpose timer</i>	YES	
<i>wlan</i>	YES	
<i>ADC</i>	YES	
<i>UART</i>	YES	
<i>I2C</i>	YES	
<i>SDIO/GSPI</i>	YES	
<i>USB</i>	YES	

<i>Wake pin</i>	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
<i>RTC</i>	YES	
<i>System timer</i>	YES	
<i>low precision timer</i>	YES	

## 7. Firmware Protection

### 7.1. Trust-Zone Lite

- Top 4k RAM cannot be read.
- RDP Interrupt will happen when invalid access happen.
- RDP image should be encrypted use RDP KEY,
- RDP image can only be decrypted and load to RDP RAM use IPSEC.
- KEY
  - 16B RDP key should be written to EFUSE RDP key area
  - Hidden EFUSE 0xB0~0xBF
  - Cannot read back again. (HW protect)
  - Auto-load to IPSEC when boot.
- Enable
  - Hidden EFUSE 0xC0[0].
  - Cannot be closed after open.

## 8. WIFI

### 8.1. General

- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

### 8.2. Standards Supported

- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WIFI WPS support
- WIFI Direct support
- Light Weight TCP/IP protocol

### 8.3. WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism

## 8.4. WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Fast receiver Automatic Gain Control (AGC)

## 9. Basic timer

### 9.1. Introduction

The basic timers TIM0/TIM1/TIM2/TIM3 consist of a 32-bit auto-reload counter without prescaler.

They may be used as generic timers for time-base generation.

### 9.2. Features

Table 9-1 Basic timer features

<b>Name</b>	<b>TIM0/1/2/3</b>
<i>channels</i>	1
<i>clock source</i>	32k
<i>resolution</i>	32bit
<i>prescaler</i>	8bit
<i>counter mode</i>	Up
<i>one pulse mode</i>	-
<i>PWM mode with polarity selection</i>	-
<i>statistic pulse width</i>	-
<i>statistic pulse number</i>	-
<i>interrupt generation</i>	●
<i>DMA generation</i>	-
<i>input pin</i>	-
<i>output pin</i>	-

## 10. Capture timer

### 10.1. Introduction

The Capture timer (TIM4) consists of a 16-bit auto-reload counter driven by a 8-bit programmable prescaler.

It may be used for a variety of purposes, including measuring the pulse lengths or numbers of input signals.

### 10.2. Features

Table 10-1 Capture timer features

<i>Name</i>	<i>TIM4</i>
<i>channels</i>	1
<i>clock source</i>	XTAL
<i>resolution</i>	16bit
<i>prescaler</i>	8bit
<i>counter mode</i>	Up
<i>one pulse mode</i>	-
<i>PWM mode with polarity selection</i>	-
<i>statistic pulse width</i>	•
<i>statistic pulse number</i>	•
<i>interrupt generation</i>	•
<i>DMA generation</i>	•
<i>input pin</i>	1 input capture
<i>output pin</i>	-



## 11. PWM timer

### 11.1. Introduction

The PWM timer (TIM5) consists of a 16-bit auto-reload counter driven by a 8-bit programmable prescaler.

It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (PWM).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler.

### 11.2. Features

Table 11-1 PWM timer features

<i>Name</i>	<i>TIM5</i>
<i>channels</i>	6
<i>clock source</i>	XTAL
<i>resolution</i>	16bit
<i>prescaler</i>	8bit
<i>counter mode</i>	Up
<i>one pulse mode</i>	●
<i>PWM mode with polarity selection</i>	●
<i>statistic pulse width</i>	-
<i>statistic pulse number</i>	-
<i>interrupt generation</i>	●
<i>DMA generation</i>	●
<i>input pin</i>	1 input capture
<i>output pin</i>	6 PWM out

### 11.3. Function description

#### 11.3.1. PWM mode

Pulse Width Modulation mode allows you to generate a signal with a frequency determined by the value of the TIMx\_ARR register and a duty cycle determined by the value of the CCRx field of TIMx\_CCRx register.

$$\text{Period} = (\text{ARR} + 1) * T_{CNT}$$

$$\text{Duty cycle: } D_{PWM} = \frac{(CCR_x + 1) * T_{CNT}}{T_{PWM}}$$

$$\text{Where } T_{CNT} = T_{XTAL} * (PSC + 1)$$

The PWM mode can be selected independently on each channel (one PWM per OCx output) by setting '0' in the OCxM bits in the TIMx\_CCRx register. You must enable the corresponding preload register by setting the OCxPE bit in the TIMx\_CCRx register, and eventually the auto-reload preload register by setting the ARPE bit in the TIMx\_CR register.

As the preload registers are transferred to the shadow registers only when an update event occurs, before starting the counter, you have to initialize all the registers by setting the UG bit in the TIMx\_EGR register.

OCx polarity is software programmable using the CCxP bit in the TIMx\_CCRx register. It can be programmed as active high or active low.

In PWM mode, TIMx\_CNT and CCRx (in TIMx\_CCRx) are always compared to determine whether  $TIMx\_CNT \leq CCRx$  (in TIMx\_CCRx). The PWM signal OCx is active as long as  $TIMx\_CNT \leq CCRx$  (in TIMx\_CCRx), otherwise it becomes inactive.

The timer is only able to generate PWM in edge-aligned mode.

## 12. RTC

### 12.1. Introduction

The real-time clock (RTC) is an independent BCD timer/counter.

One 32-bit registers contain the seconds, minutes, hours (12 or 24-hour format) expressed in binary coded decimal format (BCD).

One 32-bit registers contain the days expressed in binary format.

Daylight saving time compensation can also be performed.

Additional two 32-bit registers contain the programmable alarm seconds, minutes, hours and days.

A digital calibration feature is available to compensate for some deviation.

After backup domain reset, all RTC registers are protected against possible parasitic write accesses.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low power mode or under reset).

### 12.2. Features

- Time with seconds, minutes, hours, days (12 or 24-hour format).
- Daylight saving compensation programmable by software.
- One programmable alarm with interrupt function. The alarms can be triggered by any combination of the time fields.
- Maskable interrupts/events:
  - - Alarm
- Digital calibration circuit
- Register write protection

### 12.3. Clock and Prescalers

A programmable prescaler stage generates a 1 Hz clock which is used to update the calendar. To minimize power consumption, the prescaler is split into 2 programmable prescalers.

A 9-bit asynchronous prescaler configured through the PREDIV\_A bits of the RTC\_PRER register.

A 9-bit synchronous prescaler configured through the PREDIV\_S bits of the RTC\_PRER register.

Note: It is recommended to configure the asynchronous prescaler to a high value to minimize consumption.

Default, the asynchronous prescaler division factor is set to 128, and the synchronous division factor to 256, to obtain an internal clock frequency of 1 Hz (ck\_spre) with 32.768 kHz as RTCLK

$f_{clk\_apre}$  is given by the following formula:

$$f_{clk\_apre} = \frac{f_{RTCLK}}{PREDIV\_A + 1}$$

$f_{clk\_spre}$  is given by the following formula:

$$f_{clk\_spre} = \frac{f_{clk\_apre}}{PREDIV\_S + 1}$$

## 12.4. RTC Reset

	<i>RTC Reset</i>	<i>RTC Wakeup</i>
<i>Power Off</i>	Y	N/A
<i>Hardware Reset</i>	Y	N/A
<i>Deep Sleep</i>	Y	N/A
<i>Deep Standby</i>	N	Y
<i>Sleep</i>	N	Y
<i>System Reset</i>	N	N/A
<i>Vector Reset</i>	N	N/A

## 13. BACKUP Register

### 13.1. Introduction

The backup register are 32-bits registers used store 32 bytes of user application data, Backup registers are not reset by a system, or when the device wakes up from the Standby mode.

byte0~byte3 are reserved for system, and byte4~byte31 are reserved for user.

### 13.2. BACKUP Register API

<i>Backup Register API</i>	<i>Introduction</i>
< BKUP_Write >	■ backup register dwrod write
< BKUP_Read >	■ backup register dwrod read
< BKUP_Set >	■ set some bits of backup register
< BKUP_Clear >	■ clear some bits of backup register

### 13.3. BACKUP Register Reset

	<i>RTC Reset</i>
<i>Power Off</i>	Y
<i>Hardware Reset</i>	Y
<i>Deep Sleep</i>	Y
<i>Deep Standby</i>	N
<i>Sleep</i>	N
<i>System Reset</i>	N
<i>Vector Reset</i>	N

## 14. UART

### 14.1. Introduction

The Universal Asynchronous Receiver Transmitter (UART) module offers a flexible means of full duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

It offers a very wide range of baud rates using a fractional baud rate generator.

Low power Rx mode is implemented by monitoring Rx baud rate error and own frequency drift.

This chip integrates three UART modules:

- 2 normal UART with low power or high speed.
- 1 LOGUART with high speed.

### 14.2. Features

- Support UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bit
- Support a very wide range of baud rate, 110~6Mbps.
- APB3 bus interface
- Support DMA mode
- Support auto flow control
- Support interrupt control
- Support IrDA
- Support loopback mode for test
- Differentiate clk for Tx path and Rx path
- Fractional baud rate generator for Tx path and Rx path
- Support low power Rx path without XTAL & PLL, Baud rate 110~500000.
- Monitor and eliminate Rx baud rate error and own frequency drift automatically for new Rx path
- Transmit and Receive Data FIFO
- Programmable Receive Data FIFO Trigger Level

### 14.3. Baud Rate

Table 14-1 UART Baud Rate

	<i>High Rate</i>	<i>Low Power</i>
<i>clock select</i>	40MHz XTAL	8MHz

supported baud rate(bps)	1200, 9600, 14400, 19200, 28800, 38400, 57600, 76800, 115200, 128000, 153600, 230400, 406800, 500000, 921600, 1000000, 1382400, 1444400, 1500000, 1843200, 2000000, 2100000, 2764800, 3000000, 3250000, 3692300, 3750000, 4000000, 6000000	1200, 9600, 14400, 19200, 28800, 38400, 57600, 76800, 115200, 128000, 153600, 230400, 406800, 500000
--------------------------	--	---

## 14.4. UART Interface Signal Levels

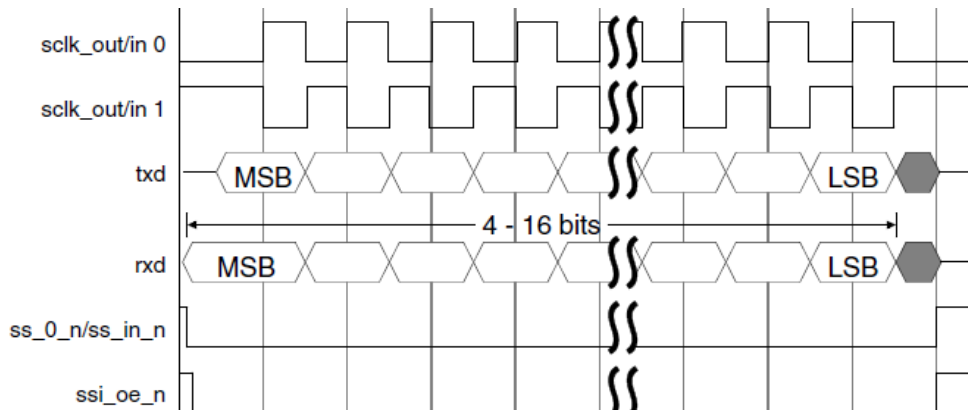
The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the Ameba-Z UART interface via the IO power.

## 15. SPI

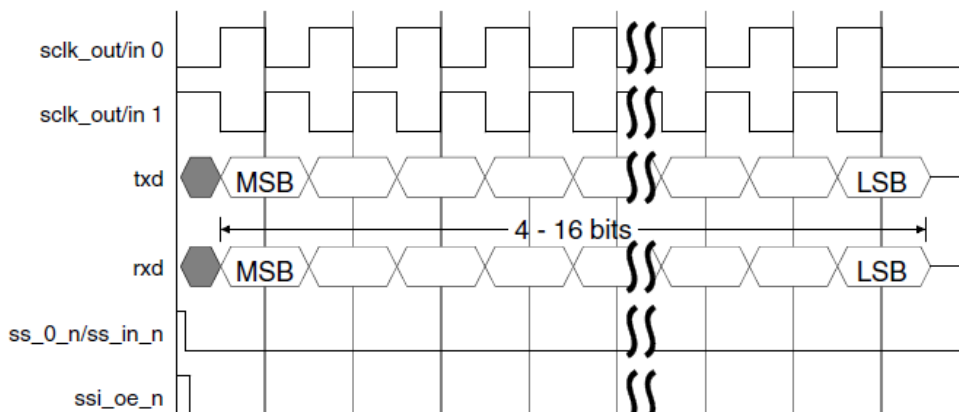
### 15.1. Introduction

Ameba-Z support Motorola Serial Peripheral Interface (SPI) – A four-wire, full-duplex serial protocol from Motorola.

There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of the slave select signal or the first edge of the serial clock.



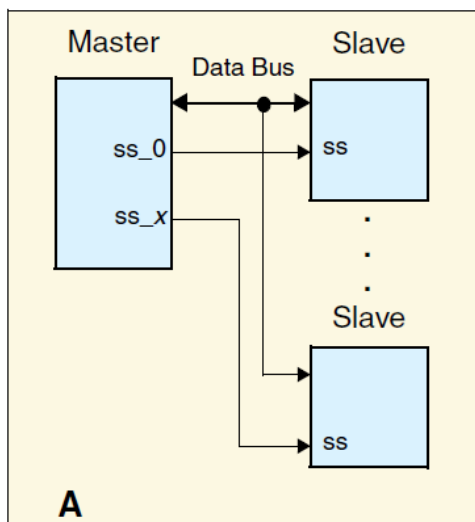
**Figure 12 SPI Serial Format (SCPH = 0)**



**Figure 13 SPI Serial Format (SCPH = 1)**

The slave select line is held high when the SPI is idle or disabled.





ss = slave select line

**Figure 14 Slave Selection**

## 15.2. Features

- Motorola SPI Interface Operations support
- Support maximum 2 SPI port
- Support Master (SPI1 only), and Slave(SPI0 only) mode
- Support DMA to offload CPU bandwidth
- high speed SPI with baud rate up to 31.25MHz
- Programmable clock bit-rate
- Programmable clock polarity and phase
- Master just support 1 hardware CS, you can use GPIO to control more SPI salve.

## 16. I2C

### 16.1. Introduction

The I2C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL).

When the bus is idle, both the SCL and SDA signals are pulled high through internal pull-up resistors. When the master wants to start a transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is 1. When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the SDA line while SCL is 1. When data is being transmitted on the bus, the SDA line must be stable when SCL is 1.

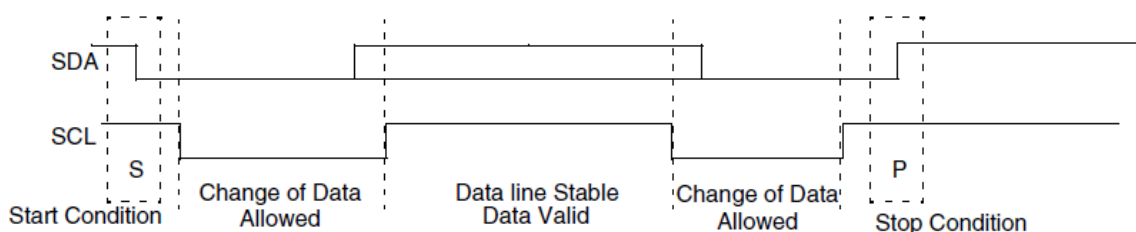


Figure 15 I2C start stop condition

I2C bus carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device.

Devices can also be considered as masters or slaves when performing data transfers. A master is a device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

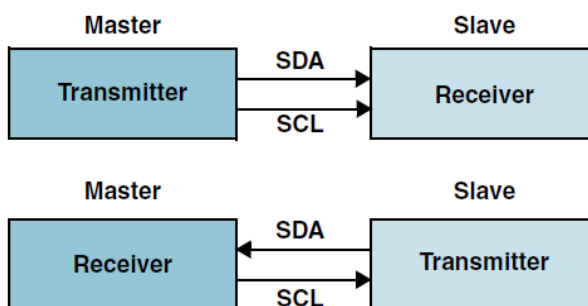
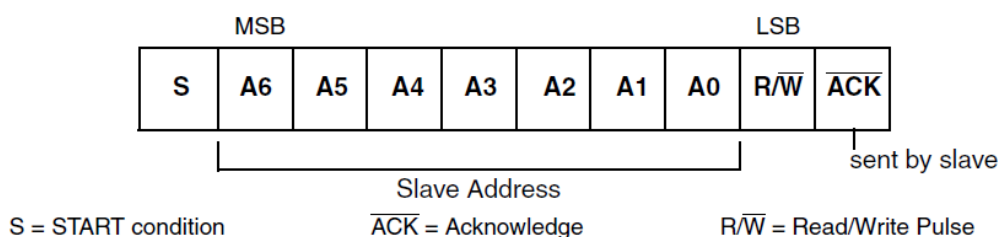
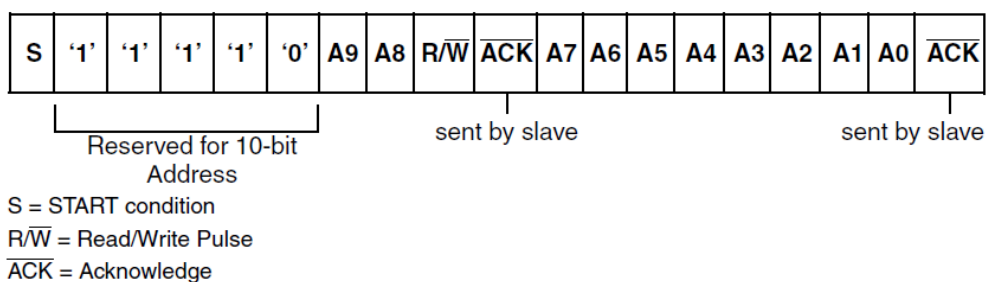


Figure 16 Master/Slave and Transmitter/Receiver Relationships

Ameba-Z can operate in standard mode (with data rates 0 to 100 Kb/s), fast mode (with data rates less than or equal to 400 Kb/s), high-speed mode (with data rates less than or equal to 3.4 Mb/s) are not supported.

Ameba-Z can communicate with devices only of these modes as long as they are attached to the bus. Additionally, fast mode devices are downward compatible. For instance, fast mode devices can communicate with standard mode devices in 0 to 100 Kb/s I2C bus system. However, standard mode devices are not upward compatible and should not be incorporated in a fast-mode I2C bus system as they cannot follow the higher transfer rate and unpredictable states would occur.

There are two address formats: the 7-bit address format and the 10-bit address format.

**7-bit Address Format**

**Figure 17 7-bit address format**
**10-bit Address Format**

**Figure 18 10-bit address format**

## 16.2. Features

- Support maximum 2 I2C port
- Two speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (<400 Kb/s)
  - Not support High-speed mode (<3.4 Mb/s)
- Master or Slave I2C operation
- 7- or 10-bit addressing
- Transmit and receive buffers
- TX and RX DMA support
- Slave mode address match wakeup for power save

## 17. I2S

### 17.1. Introduction

I2S (Inter IC Sound) is a standard communication structure using in digital audio systems. Since the digital audio signals in consumer audio market are being processed by a number of VLSI ICs, standardized communication structure could increase system flexibility.

### 17.2. Features

- Sample bit: 16 bit , 24 bit
- Sample rate: 8K, 16K, 24K, 32K, 48K, 96K, 7.35K, 14.7K, 22.05K, 29.4K, 44.1K, 88.2K
- IIS throughput: 0.512Mbps (16K\*32bit) ~ 6.144Mbps (96K\*64bit)
- IIS channel number: mono, stereo
- Integrated DMA engine to minimize SW efforts
- Master or slave mode support
- Support Mono and Stereo TX or RX or TX&RX mode
- Not support PCM mode

### 17.3. Function Description

#### 17.3.1. Clock Type

- SCLK : 6.144MHz, 3.072MHz, 2.048Mz, 1.536MHz, 1.024MHz ,0.512MHz,0.256MHZ
- MCLK :24.576Mhz, 12.288Mz, 8.192MHz, 6.144MHz , 4.096Mhz , 2.048Mhz
- WS(Sample Rate): 96K, 48K, 32K, 24K, 16K, 8K ( )
- MCLK=4SCLK=256WS (24bit)
- MCLK=8SCLK=256WS (16bit)

## 18. ADC

### 18.1. Introduction

Ameba-Z integrates one ADC with as many as four channels: One internal channel and three external channels.

### 18.2. Features

<i>Item</i>	<i>Spec.</i>	<i>Description</i>
<b>Channel</b>	4 independent channels	1 internal channel 3 external channels
<b>Input Power</b>	0~3.3V or 0~5V	CH1 & CH3: 0~3.3V CH2: 0~5V
<b>Input Signal Bandwidth</b>	<60Hz	
<b>Resolution</b>	12-bits	Bit Number
<b>DMA Mode</b>	Support	
<b>One Shot Mode</b>	Support	Support Timer(TIM3) trigger one shot sampling without CPU active for save power
<b>Sample Rate</b>	Max. 1MHz per channel, Configurable	Sampling frequency
<b>Wakeup Method</b>	buffer threshold and event trigger	

### 18.3. Channel Description

	<i>Internal</i>	<i>PinName</i>	<i>Voltage</i>
<b>CH0</b>	Y	N/A	N/A
<b>CH1</b>	N	GPIOA19/ADC_1	0~3.3V
<b>CH2</b>	N	VBAT_MEAS	0~5V
<b>CH3</b>	N	GPIOA_20/ADC_3	0~3.3V

## 19. GDMA

### 19.1. Introduction

General purpose direct memory access (GDMA) is used to transfer data between peripherals and memory as well as memory to memory without CPU actions.

Ameba-Z integrate two GDMA modules, One GDMA module has 6 channels to manage the data transfer between memory and peripherals.

### 19.2. Features of GDMA

- Dual port DMA with totally 12 channels
- Single FIFO per channel for source and destination
- Support memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral DMA transfer
- Support multi block transfer
- Maximum block size is 4095
- Programmable source and destination addresses; address increment, decrement, no change or address auto-reload
- Configurable endian
- Support block level flow control
- DMA interrupt for complete or error

## 20. WGT (watchdog timer)

### 20.1. Introduction

The watchdog timer regains control in case of system failure (due to a software error) to increase application reliability. The WDT can generate a reset or an interrupt when the counter reaches a given timeout value.

### 20.2. Features

- Watch dog timer is count with  $32.768\text{KHz}/(\text{divfactor}+1)$ . Dividing factor is  $1\sim 0\text{xFFFF}$ .
- Timeout value: 1ms ~ 8190s
- Configurable reset or interrupt generation with the given timeout value
- Watch dog timer disable/enable/refresh

## 21. GPIO

### 21.1. Introduction

Ameba-Z GPIO IP controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.

Ameba-Z support two port: PORT\_A(0~31) and PORT\_B(0~6).

Port A can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge

NOTICE: Both edge interrupt is not support.

The interrupts can be masked by programming the `gpio_int_mask` register. The interrupt status can be read before masking (called raw status) and after masking.

Whenever Port A is configured for interrupts, the data direction must be set to Input. If the data direction register is reprogrammed to Output, then any pending interrupts are not lost. However, no new interrupts are generated.

If the user has configured Port A to include the interrupt feature, the GPIO can be configured to either include or exclude a debounce capability using the `GPIO_DEBOUNCE` parameter.

The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.

### 21.2. Features of GPIO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions
- `GPIO_DEBOUNCE` to remove any spurious glitches



## 22. Security Engine

### 22.1. Introduction

The Security engine provides fast and energy efficient hardware encryption and decryption service for Ameba-Z.

### 22.2. Features

- Provide low SW computing and high performance encryption
- Efficient CPU/DMA access support
- Block size up to 32KB.
- Supported authentication algorithms:
  - MD5
  - SHA-1
  - SHA-2 (SHA-224 / SHA-256 )
  - HMAC-MD5
  - HMAC-SHA1
  - HMAC-SHA2
- Supported Encryption / Decryption mechanisms:
  - DES ( CBC / ECB )
  - 3DES ( CBC / ECB )
  - AES-128 ( CBC / ECB / CTR )
  - AES-192 ( CBC / ECB / CTR )
  - AES-256 ( CBC / ECB / CTR )

## 23. USOC (USB device)

### 23.1. Introduction

USOC is USB device controller that is compliant with the USB 2.0 specification.

The USOC module connects SIE to AHB system bus so that USB can work in two modes:

- iNIC mode, all SIE data transfer is through AHB bus.
- NIC mode or Dongle mode, all SIE data transfer is through legacy TDE/RDE interface.

In two modes, register access path are all enabled to get the highest flexibility to configure SIE, or other system block such as WLON/SYSON.

### 23.2. Features

- Support USB 2.0
- Support HS/FS/LS mode
- Internal DMA support, DMA works based on register settings
- Support high performance Ethernet to WIFI transformation
- Support non-flash booting in the use if Ethernet to WIFI transformation card
- 1.5KByte bulk-in buffer and 1.5KByte bulk-out buffer
- Switch NIC and iNIC mode by register settings
- Interrupt mitigation
- Error handling
- Support Mass storage and network device

## 24. SDIO/GSPI device

### 24.1. Introduction

The SDIO Controller supports the Secure Digital I/O communication protocol and Realtek SPI protocol.

### 24.2. Features

- Support SDIO 2.0 SDR25
- CIS can be configured with internal non-volatile memory for fast card detection
- Realtek SPI provides high efficiency SPI interface with interrupt and full duplex mode
- Support high performance Ethernet to WIFI transformation
- Support non-flash booting in the use if Ethernet to WIFI transformation card
- Clock rate variable up to 50 MHz
- Internal DMA support

### 24.3. Bus Timing Specification

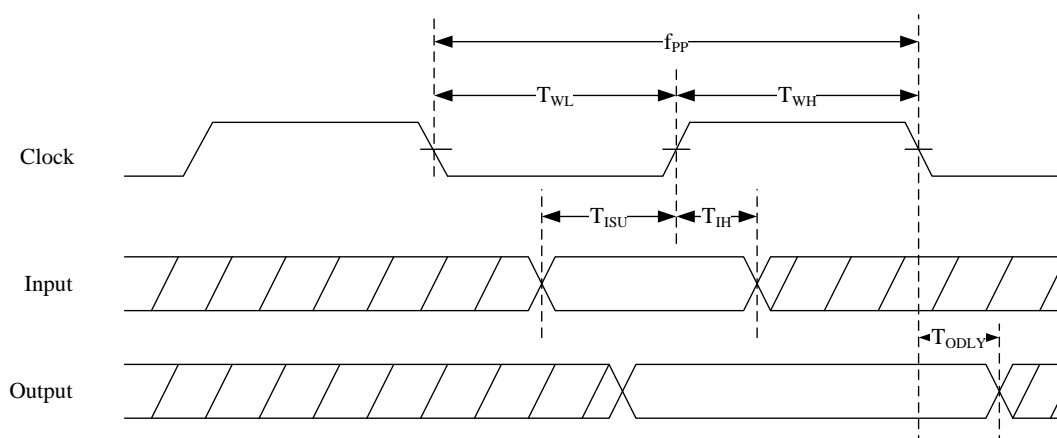


Figure 19 SDIO bus timing

Table 24-1 SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
$f_{PP}$	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
$T_{WL}$	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns

$T_{WH}$	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
$T_{ISU}$	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
$T_{IH}$	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
$T_{ODLY}$	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns



## 25. Electrical Characteristics

### 25.1. Temperature Limit Ratings

**Table 25-1 Temperature Limit Ratings**

<i>Parameter</i>	<i>Minimum</i>	<i>Maximum</i>	<i>Units</i>	<i>Comment</i>
<b>Storage Temperature</b>	-55	+125	°C	
<b>Ambient Operating Temperature</b>	-20	+85	°C	<i>RTL8710BX-VT1-CG can support -40~105(*)</i>
<b>Junction Temperature</b>	0	+125	°C	

\* Guaranteed by design

### 25.2. Power Supply DC Characteristics

**Table 25-2 Power Supply DC Characteristics**

<i>Symbol</i>	<i>Parameter</i>	<i>Minimum</i>	<i>Typical</i>	<i>Maximum</i>	<i>Units</i>
<b>VA33, VD33IO, SW_HV3</b>	3.3V Supply Voltage	3.0	3.3	3.6	V
<b>VDD_IO</b>	Digital IO Supply Voltage	1.62	1.8~3.3	3.6	V
<b>VA12_AFE, VA12_SYN, VA12_RF</b>	1.2V Core Supply Voltage	1.08	1.2	1.32	V
<b>IDD33</b>	3.3V Rating Current (with internal regulator and integrated CMOS PA)	-	-	450	mA
<b>IDD_IO</b>	IO Rating Current (including VDD_IO)			200	mA
<b>IDD_IO_33</b>	3.3V IO Rating Current			50	mA

### 25.3. Digital IO Pin DC Characteristics

#### 25.3.1. Electrical Specifications

**Table 25-3 Typical Digital IO DC Parameters (3.3V Case)**

<i>Symbol</i>	<i>Parameter</i>	<i>Conditions</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>	<i>Units</i>
<b>V<sub>IH</sub></b>	Input-High Voltage	LVTTTL	2.0	-	-	V

$V_{IL}$	Input-Low Voltage	LVTTTL	-	-	0.8	V
$V_{OH}$	Output-High Voltage	LVTTTL	2.4	-	-	V
$V_{OL}$	Output-Low Voltage	LVTTTL	-	-	0.4	V
$I_{T+}$	Schmitt-trigger High Level		1.78	1.87	1.97	V
$I_{T-}$	Schmitt-trigger Low Level		1.36	1.45	1.56	V
$I_{IL}$	Input-Leakage Current	$V_{IN}=3.3V$ or 0	-10	$\pm 1$	10	$\mu A$

**Table 25-4 Typical Digital IO DC Parameters (1.8V Case)**

<i>Symbol</i>	<i>Parameter</i>	<i>Conditions</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>	<i>Units</i>
$V_{IH}$	Input-High Voltage	CMOS	0.65x Vcc	-	-	V
$V_{IL}$	Input-Low Voltage	CMOS	-	-	0.35x Vcc	V
$V_{OH}$	Output-High Voltage	CMOS	Vcc-0.45	-	-	V
$V_{OL}$	Output-Low Voltage	CMOS	-	-	0.45	V
$I_{T+}$	Schmitt-trigger High Level		1.02	1.09	1.14	V
$I_{T-}$	Schmitt-trigger Low Level		0.67	0.73	0.87	V
$I_{IL}$	Input-Leakage Current	$V_{IN}=1.8V$ or 0	-10	$\pm 1$	10	$\mu A$

## 26. Mechanical Dimensions

### 26.1. Package Specification

#### 26.1.1. QFN32

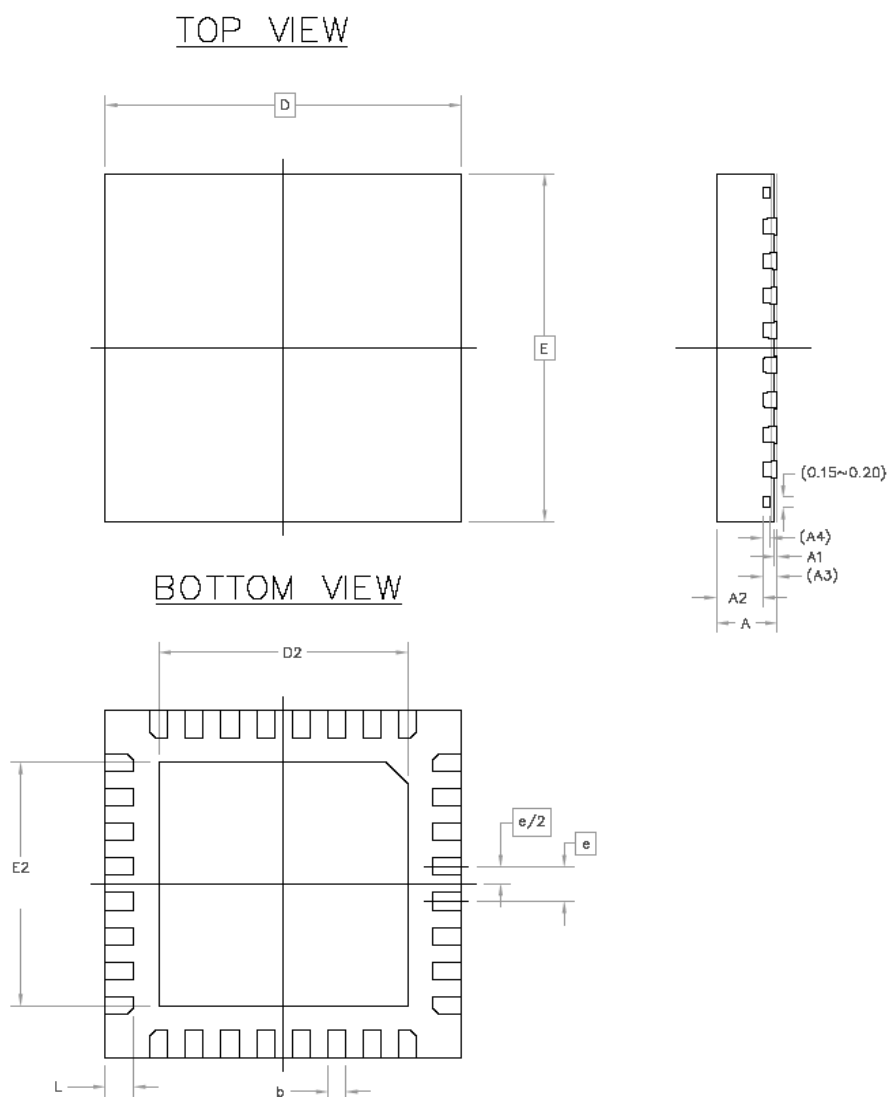


Figure 20 QFN32 Package Specification

Table 26-1 QFN32 Package Specification

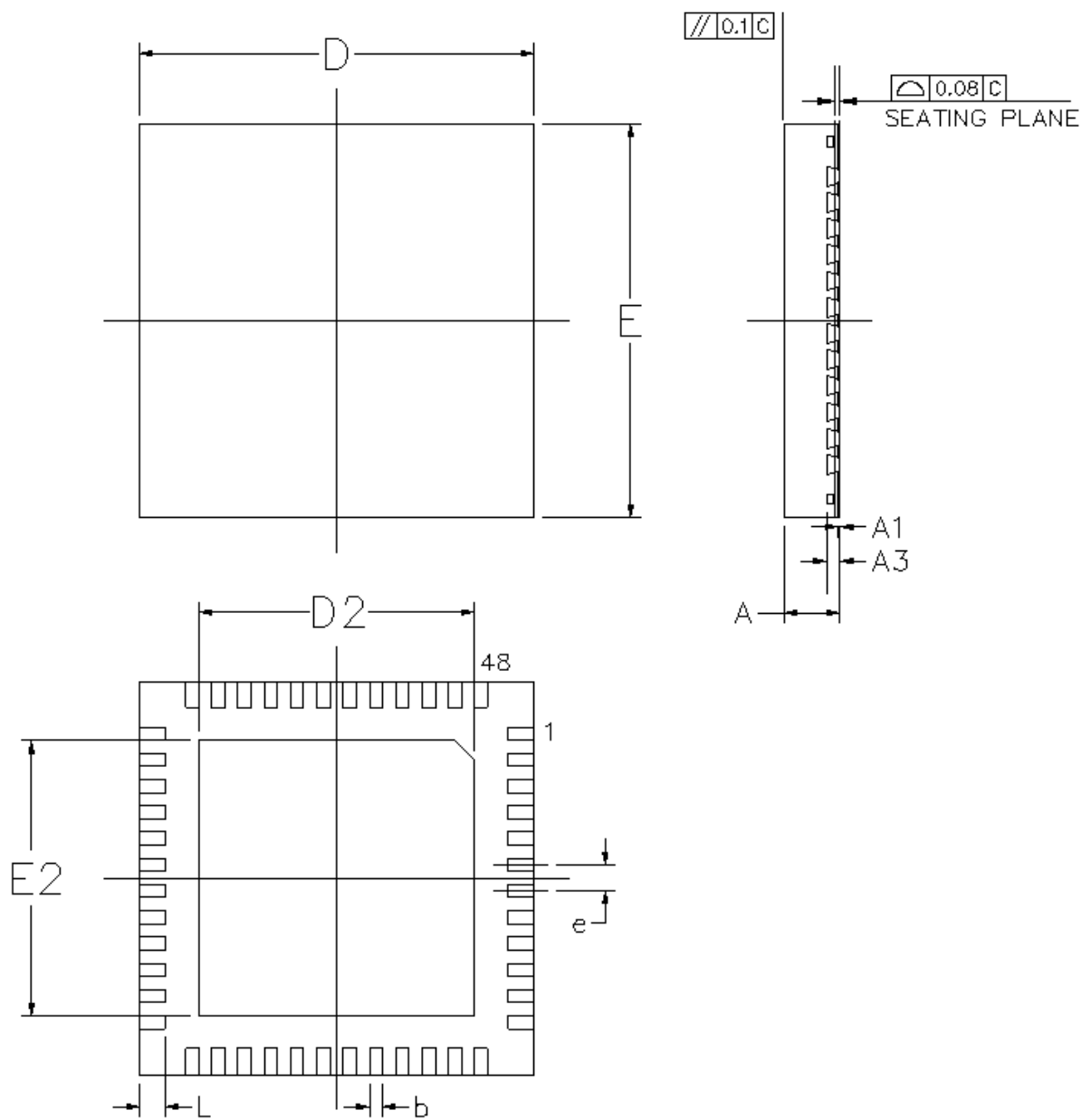
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035



<b>A1</b>	0.00	0.02	0.05	0.000	0.001	0.002
<b>A3</b>	0.20 REF			0.008 REF		
<b>A4</b>	0.10 REF			0.004 REF		
<b>b</b>	0.18	0.25	0.30	0.007	0.010	0.012
<b>D/E</b>	5.00 BSC			0.020 BSC		
<b>D2/E2</b>	3.25	3.50	3.75	0.128	0.138	0.148
<b>e</b>	0.50 BSC			0.020 BSC		
<b>L</b>	0.30	0.40	0.50	0.012	0.016	0.020

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

**26.1.2. QFN48**

**Figure 21 QFN48 Package Specification**
**Table 2 QFN48 Package Specification**

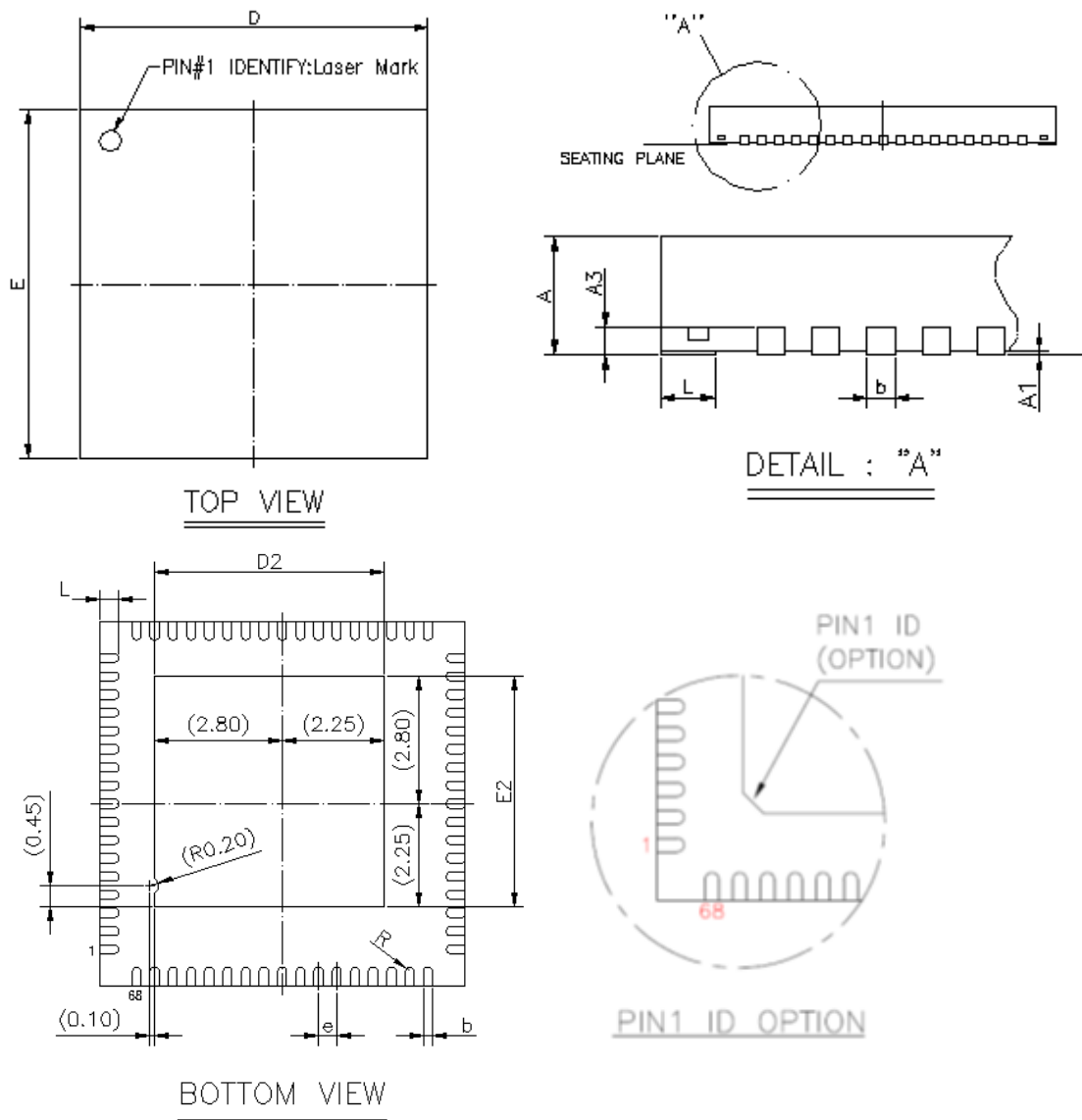
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.75	0.85	1.00	0.030	0.034	0.039

<b>A<sub>1</sub></b>	0.00	0.02	0.05	0.000	0.001	0.002
<b>A<sub>3</sub></b>	0.20 REF			0.008 REF		
<b>b</b>	0.15	0.20	0.25	0.006	0.008	0.010
<b>D/E</b>	6.00BSC			0.236BSC		
<b>D<sub>2</sub>/E<sub>2</sub></b>	4.0	4.2	4.5	0.157	0.167	0.177
<b>e</b>	0.40BSC			0.016BSC		
<b>L</b>	0.30	0.40	0.50	0.012	0.016	0.020

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).

REFERENCE DOCUMENTL : JEDEC MO-220.

**26.1.3. QFN68**

**Figure 22 QFN68 Package Specification**
**Table 26-3 QFN68 Package Specification**

<b>Symbol</b>	<b>Dimension in mm</b>			<b>Dimension in inch</b>		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.80	0.85	0.90	0.031	0.033	0.035
<b>A<sub>1</sub></b>	0.00	0.02	0.05	0.000	0.001	0.002

<b>A<sub>3</sub></b>	<b>0.2 REF</b>			<b>0.008 REF</b>		
<b>b</b>	0.15	0.20	0.25	0.006	0.008	0.010
<b>D/E</b>	7.90	8.00	8.10	0.311	0.315	0.319
<b>D<sub>2</sub>/E<sub>2</sub></b>	4.95	5.05	5.15	0.195	0.199	0.203
<b>e</b>	<b>0.40 BSC</b>			<b>0.016 BSC</b>		
<b>L</b>	0.30	0.40	0.50	0.012	0.016	0.020

**Notes :**

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.