



# REALTEK

**ALC883-GR**  
**ALC883DD-GR**

**7.1+2 CHANNEL HIGH DEFINITION AUDIO CODEC**

## **DATASHEET**

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## **USING THIS DOCUMENT**

This document is intended for the hardware and software engineer’s general information on the Realtek ALC883 Series Audio Codec ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

## **REVISION HISTORY**

| <b>Revision</b> | <b>Release Date</b> | <b>Summary</b>                                                                                                                                                        |
|-----------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.0             | 2005/08/02          | First release.                                                                                                                                                        |
| 1.1             | 2005/08/22          | Update section 2.1 Hardware Features, page 2, section 9.1.1 Absolute Maximum Ratings, page 61, and section 12 Ordering Information, page 70.                          |
| 1.2             | 2006/04/03          | Add a note to section 9.1.1 Absolute Maximum Ratings, page 61.<br>Update Table 4, page 8, and Table 77, page 65.<br>Revised section 12 Ordering Information, page 70. |

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## 1. General Description

The ALC883\* series 7.1+2 Channel High Definition Audio (HDA) codecs are compliant with Microsoft's UAA (Universal Audio Architecture). The ALC883 series provide 10 DAC channels that simultaneously support 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel stereo output. Flexible mixing, mute, and fine gain control functions provide a complete integrated audio solution for home entertainment PCs.

The ALC883 series also integrates two stereo ADCs that can support a stereo microphone with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technology simultaneously.

All analog IOs are input and output capable, and headphone amplifiers are also integrated at each analog output. All analog IOs can be re-tasked according to user's definitions, or automatically switched depending on the connected device type.

The ALC883 supports 16/20/24 S/PDIF input and output to offer easy connection of PCs to high quality consumer electronic products such as digital decoders and speakers.

The ALC883 series supports host/soft audio from the Intel ICH series chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and renowned software utilities like Karaoke mode, environment emulation, software equalizer, HRTF 3D positional audio, and optional Dolby® Digital Live and DTS® CONNECT™, the ALC883 series provides an excellent entertainment package and game experience for PC users.

*\*Note: The ALC883 series covers all products listed in section 12 Ordering Information, page 70.*

## 2. Features

### 2.1. *Hardware Features*

- High-performance DACs with 95dB SNR (A-Weighting), ADCs with 85dB SNR (A-Weighting)
- Meets performance requirements for audio on PC2001 systems and Microsoft WLP 2.x
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel output
- 2 stereo ADCs support 16/20/24-bit PCM format, one for stereo microphone, one for legacy mixer recording
- All DACs supports 44.1K/48K/96K/192kHz sample rate
- All ADCs support 44.1K/48K/96K sample rate
- 16/20/24-bit S/PDIF-OUT supports 44.1K/48K/96/192kHz sample rate
- 16/20/24-bit S/PDIF-IN supports 44.1K/48K/96 sample rate
- Up to four channels of microphone array input are supported for AEC/BF application
- High-quality analog differential CD input
- Supports external PCBEEP input and built-in digital BEEP generator
- Software selectable 2.5V/3.75V VREFOUT
- Two jack detection pins each designed to detect up to 4 jacks
- Reserve analog mixer architecture for backward compatibility with AC'97
- Wide range (–80dB ~ +42dB) volume control with 1.5dB resolution of analog to analog mixer gain
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built-in headphone amplifiers for each re-tasking jack
- Two GPIOs (General Purpose Input/Output) for customized applications
- Pin compatible with the ALC880 and ALC882
- Enhanced S/PDIF-IN circuitry ensures compatibility with consumer DVD players
- 48-pin LQFP ‘Green’ package

## ***2.2. Software Features***

- Meets Microsoft WHQL/WLP 2.x audio requirements
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio
- Emulation of 26 sound environments to enhance gaming experience
- 10 Band Software Equalizer
- Voice Cancellation and Key Shifting in Karaoke mode
- Realtek Media Player
- Enhanced Configuration Panel to improve user experience
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS) and Beam Forming (BF) technology for voice application
- ALC883DD-GR features Dolby® Digital Live and DTS® CONNECT™

## **3. System Applications**

- Desktop multimedia PCs
- Entertainment PCs for digital home application
- Information appliances (IA) e.g., set-top box

## 4. Block Diagram

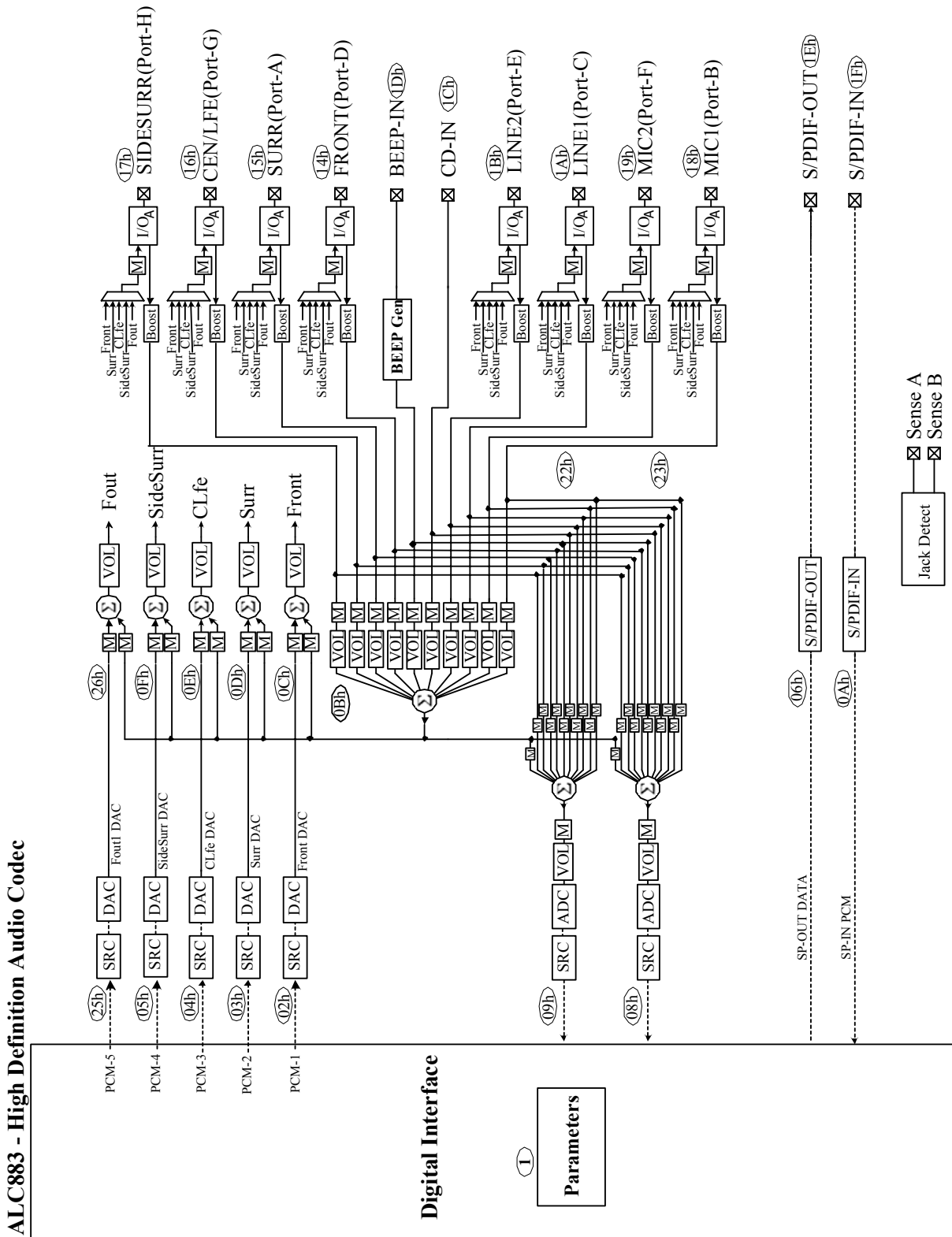


Figure 1. Block Diagram

## 4.1. Analog Input/Output Unit

Pin Complex widgets NID=14h~1Bh are re-tasking IO.

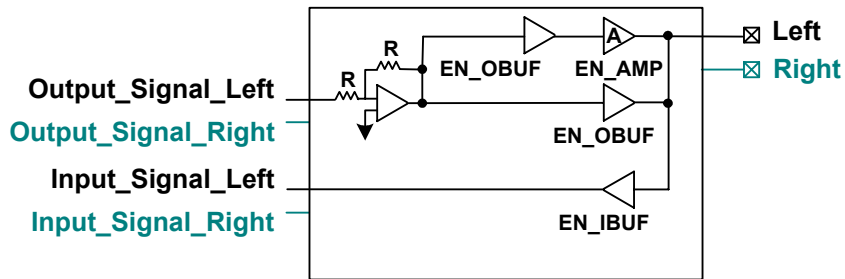


Figure 2. Analog Input/Output Unit

## 5. Pin Assignments

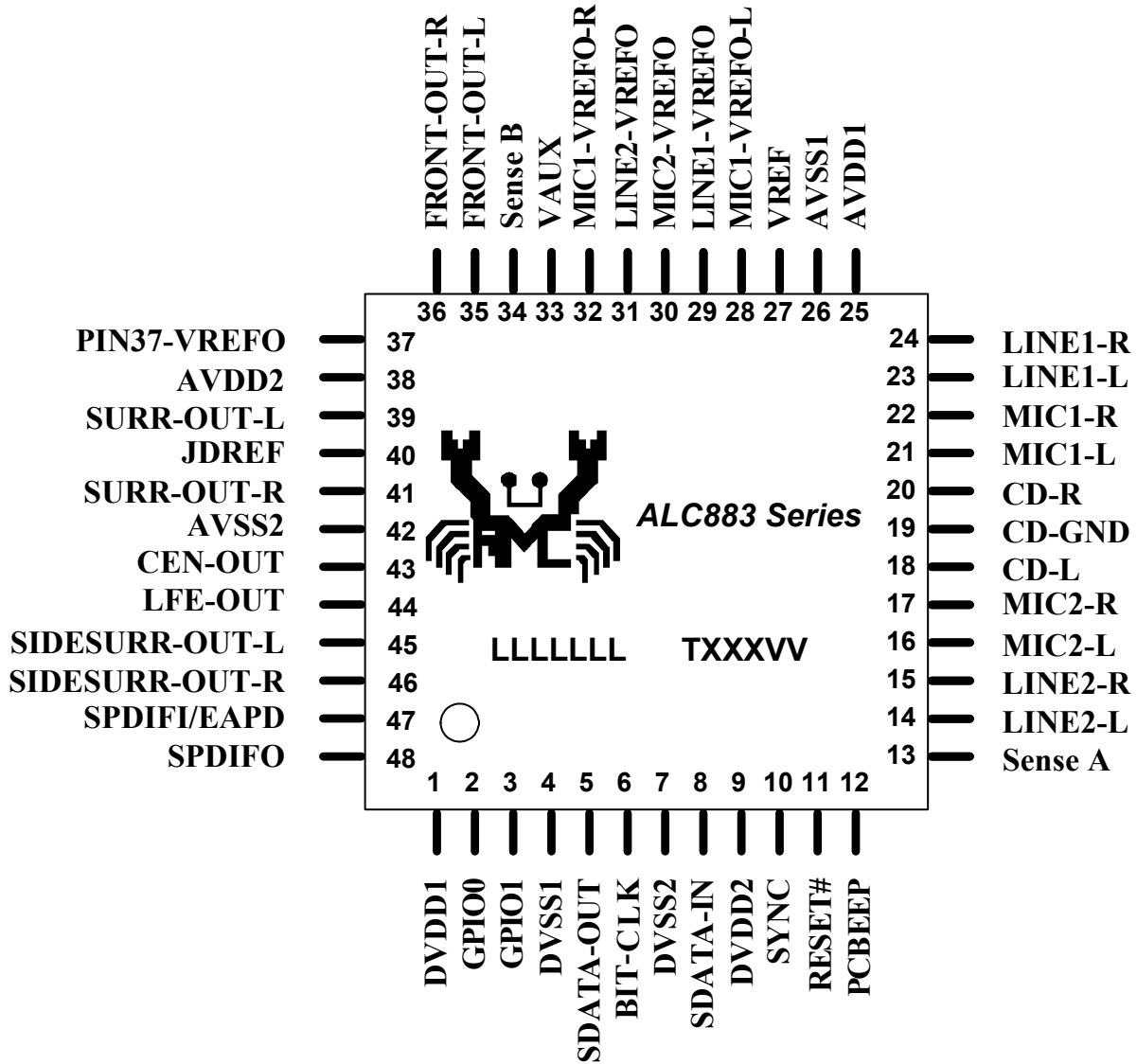


Figure 3. Pin Assignments

### 5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. The version number is shown in the location marked 'VV'.

## 6. Pin Descriptions

### 6.1. Digital I/O Pins

**Table 1. Digital I/O Pins**

| Name             | Type | Pin No. | Description                                     | Characteristic Definition                                         |
|------------------|------|---------|-------------------------------------------------|-------------------------------------------------------------------|
| RESET#           | I    | 11      | H/W reset                                       | TTL input, $V_{IL}=1.0V$ , $V_{IH}=2.0V$                          |
| SYNC             | I    | 10      | Sample Sync (48kHz)                             | Schmitt trigger input, $V_{IL}=1.0V$ , $V_{IH}=2.0V$              |
| BITCLK           | I    | 6       | 24MHz Bit clock input                           | Schmitt trigger input, $V_{IL}=1.0V$ , $V_{IH}=2.0V$              |
| SDATA-OUT        | I    | 5       | Serial TDM data input                           | TTL input, $V_{IL}=1.0V$ , $V_{IH}=2.0V$                          |
| SDATA-IN         | O    | 8       | Serial TDM data output                          | TTL output, $V_{OH}=0.9*DVDD$ , $V_{OL}=0.1*DVDD$                 |
| SPDIFI /<br>EAPD | I/O  | 47      | S/PDIF Input /<br>Signal to power down ext. amp | Schmitt input ( $V_{IL}=1.45V$ , $V_{IH}=1.85V$ ) /<br>TTL output |
| SPDIFO           | O    | 48      | S/PDIF output                                   | TTL output has 12mA@75Ω driving capability                        |
| GPIO0            | I/O  | 2       | General Purpose Input/Output 0                  | TTL input/output, $V_i=(2/3)*DVDD$ for input                      |
| GPIO1            | I/O  | 3       | General Purpose Input/Output 1                  | TTL input/output, $V_i=(2/3)*DVDD$ for input                      |
|                  |      |         |                                                 | Total: 9 Pins                                                     |

### 6.2. Analog I/O Pins

**Table 2. Analog I/O Pins**

| Name            | Type | Pin No. | Description                                              | Characteristic Definition                       |
|-----------------|------|---------|----------------------------------------------------------|-------------------------------------------------|
| LINE2-L         | IO   | 14      | 2 <sup>nd</sup> line input left channel                  | Analog input/output, default is input (JACK-E)  |
| LINE2-R         | IO   | 15      | 2 <sup>nd</sup> line input right channel                 | Analog input/output, default is input (JACK -E) |
| MIC2-L          | IO   | 16      | 2 <sup>nd</sup> stereo microphone input<br>left channel  | Analog input/output, default is input (JACK -F) |
| MIC2-R          | IO   | 17      | 2 <sup>nd</sup> stereo microphone input<br>right channel | Analog input/output, default is input (JACK -F) |
| CD-L            | I    | 18      | CD input left channel                                    | Analog input, 1.6Vrms of full scale input       |
| CD-G            | I    | 19      | CD input reference ground                                | Analog input, 1.6Vrms of full scale input       |
| CD-R            | I    | 20      | CD input right channel                                   | Analog input, 1.6Vrms of full scale input       |
| MIC1-L          | IO   | 21      | 1 <sup>st</sup> stereo microphone input<br>left channel  | Analog input/output, default is input (JACK -B) |
| MIC1-R          | IO   | 22      | 1 <sup>st</sup> stereo microphone input<br>right channel | Analog input/output, default is input (JACK -B) |
| LINE1-L         | IO   | 23      | 1 <sup>st</sup> line input left channel                  | Analog input/output, default is input (JACK -C) |
| LINE1-R         | IO   | 24      | 1 <sup>st</sup> line input right channel                 | Analog input/output, default is input (JACK -C) |
| PCBEEP          | I    | 12      | External PCBEEP input                                    | Analog input, 1.6Vrms of full scale input       |
| FRONT-<br>OUT-L | IO   | 35      | Front output left channel                                | Analog output (JACK -D)                         |
| FRONT-<br>OUT-R | IO   | 36      | Front output right channel                               | Analog output (JACK -D)                         |
| SURR-OUT-L      | IO   | 39      | Surround out left channel                                | Analog output (JACK -A)                         |
| SURR-OUT-R      | IO   | 41      | Surround out right channel                               | Analog output (JACK -A)                         |

| Name           | Type | Pin No. | Description                        | Characteristic Definition        |
|----------------|------|---------|------------------------------------|----------------------------------|
| CEN-OUT        | O    | 43      | Center output                      | Analog output (JACK -G)          |
| LFE-OUT        | O    | 44      | Low Frequency output               | Analog output (JACK -G)          |
| SIDESURR-OUT-L | O    | 45      | Side Surround output left channel  | Analog output (JACK -H)          |
| SIDESURR-OUT-R | O    | 46      | Side Surround output right channel | Analog output (JACK -H)          |
| Sense A        | I    | 13      | Jack Detect pin 1                  | Jack resistor network input 1    |
| Sense B        | I    | 34      | Jack Detect pin 2                  | Jack resistor network input 2    |
| VAUX           | -    | 33      | Standby mode control               | Pull high to enable standby mode |
|                |      |         |                                    | Total: 23 Pins                   |

### 6.3. Filter/Reference

**Table 3. Filter/Reference**

| Name                       | Type | Pin No. | Description                                                 | Characteristic Definition                  |
|----------------------------|------|---------|-------------------------------------------------------------|--------------------------------------------|
| VREF                       | -    | 27      | 2.5V Reference voltage                                      | 10uf capacitor to analog ground            |
| MIC1-VREFO-L               | O    | 28      | Bias voltage for MIC1 jack                                  | 2.5V/3.75Vreference voltage                |
| LINE1-VREFO                | O    | 29      | Bias voltage for LINE1 jack                                 | 2.5V/3.75Vreference voltage                |
| MIC2-VREFO                 | O    | 30      | Bias voltage for MIC2 jack                                  | 2.5V/3.75Vreference voltage                |
| LINE2-VREFO                | O    | 31      | Bias voltage for LINE2 jack                                 | 2.5V/3.75Vreference voltage                |
| MIC1-VREFO-R (PIN32-VREFO) | O    | 32      | Bias voltage for MIC1 jack or software select specific jack | 2.5V/3.75Vreference voltage                |
| PIN37-VREFO                | O    | 37      | software select for specific jack                           | 2.5V/3.75Vreference voltage                |
| JDREF                      | -    | 40      | Reference resistor for Jack detection                       | 20K, 1% external resistor to analog ground |
|                            |      |         |                                                             | Total: 8 Pins                              |

### 6.4. Power/Ground

**Table 4. Power/Ground**

| Name  | Type | Pin No | Description        | Characteristic Definition             |
|-------|------|--------|--------------------|---------------------------------------|
| AVDD1 | I    | 25     | Analog VDD         | Analog power for mixer and amplifier  |
| AVSS1 | I    | 26     | Analog GND         | Analog ground for mixer and amplifier |
| AVDD2 | I    | 38     | Analog VDD         | Analog power for DACs and ADCs        |
| AVSS2 | I    | 42     | Analog GND         | Analog ground for DACs and ADCs       |
| DVDD1 | I    | 1      | Digital VDD (3.3V) | Digital power                         |
| DVSS1 | I    | 4      | Digital GND        | Digital ground                        |
| DVDD2 | I    | 9      | Digital VDD (3.3V) | Digital power                         |
| DVSS2 | I    | 7      | Digital GND        | Digital ground                        |
|       |      |        |                    | Total: 8 Pins                         |

## 7. High Definition Audio Link Protocol

### 7.1. Link Signals

The High Definition Audio (HDA) link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 4 shows the basic concept of the HDA link protocol.

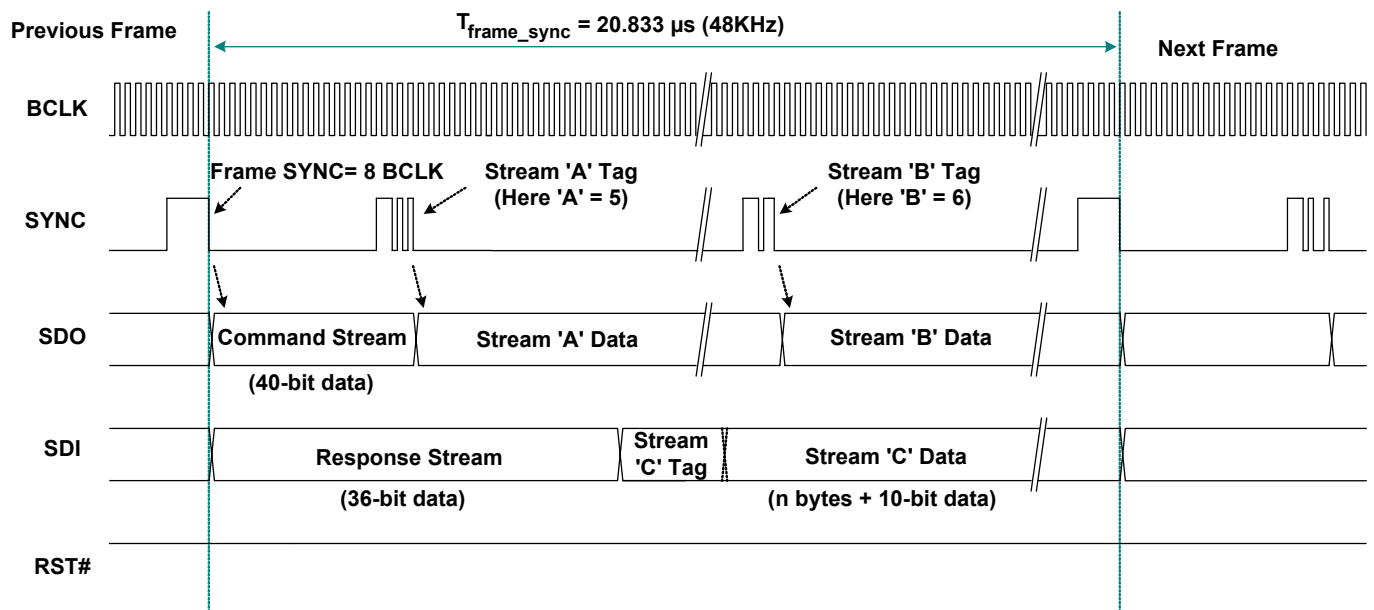


Figure 4. HDA Link Protocol

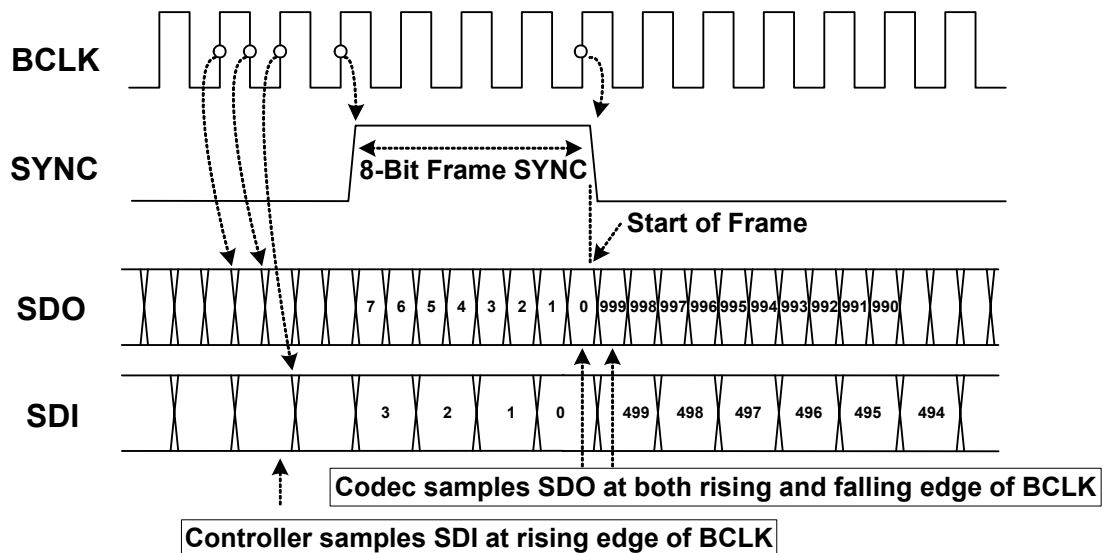
### 7.1.1. Signal Definitions

**Table 5. Link Signal Definitions**

| Item | Description                                                                                                                                                                                                                                                                                                                                                                                               |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BCLK | 24.0MHz bit clock sourced from the HDA controller and connecting to all codecs.                                                                                                                                                                                                                                                                                                                           |
| SYNC | 48kHz of signal is used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs.                                                                                                                                                                                                                                                            |
| SDO  | Serial data output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported.                     |
| SDI  | Serial data input signal driven by the codec. It is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID. |
| RST# | Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs.                                                                                                                                                                                                                                                       |

**Table 6. HDA Signal Definitions**

| Signal Name | Source           | Type for Controller | Description                                                        |
|-------------|------------------|---------------------|--------------------------------------------------------------------|
| BCLK        | Controller       | Output              | Global 24.0MHz bit clock                                           |
| SYNC        | Controller       | Output              | Global 48kHz Frame Sync and outbound tag signal                    |
| SDO         | Controller       | Output              | Serial data output from controller                                 |
| SDI         | Codec/Controller | Input/Output        | Serial data input from codec. Weakly pulled down by the controller |
| RST#        | Controller       | Output              | Global active low reset signal                                     |



### 7.1.2. Signaling Topology

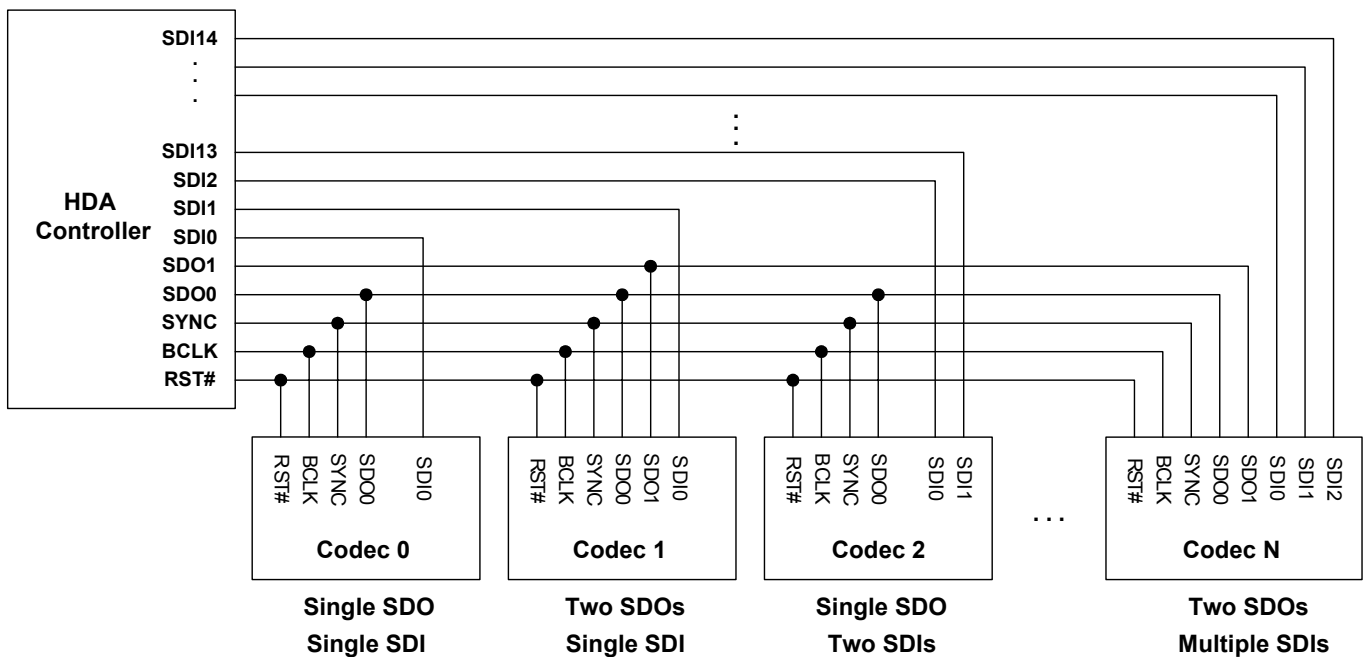
The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0 and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 6 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 12 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 6 can be implemented concurrently in an HDA system. The ALC883 series is designed to receive a single SDO stream.



**Figure 6. Signaling Topology**

## 7.2. Frame Composition

### 7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-Bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be two blocks in the same stream to carry 96kHz samples (Figure 7).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-Bit preamble and 4-Bit stream ID (Figure 8).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

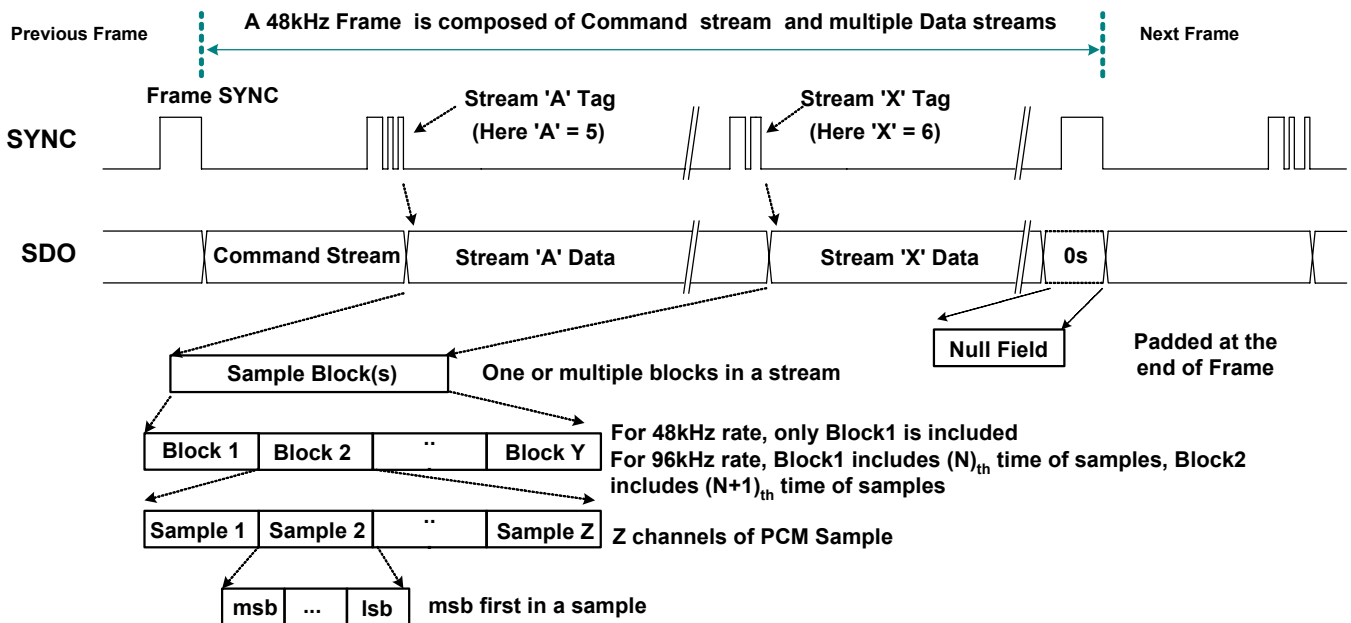


Figure 7. SDO Outbound Frame

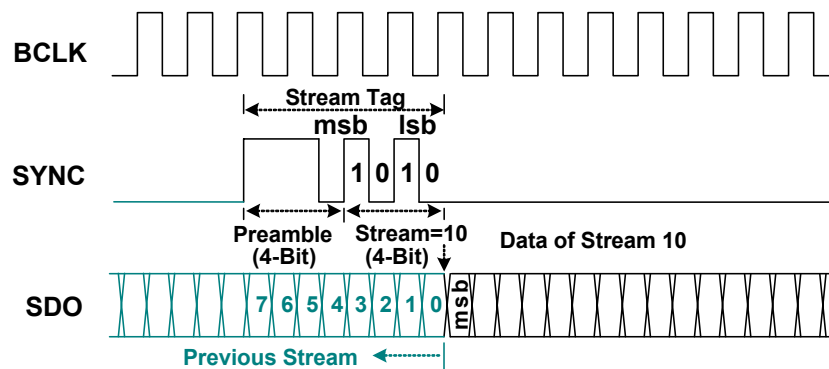


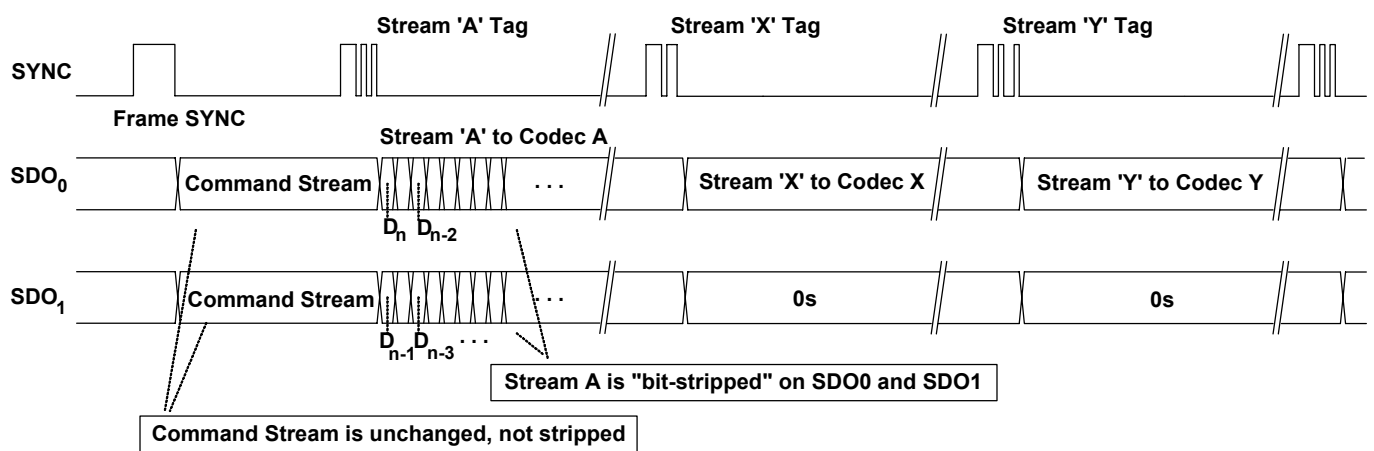
Figure 8. SDO Stream Tag is Indicated in SYNC

### 7.2.2. Outbound Frame – Multiple SDO

The HDA controller allows two SDO signals to be used to strip outbound data, completing transmission in less time to get more bandwidth. If software determines the target codec supports multiple SDO capability, it enables the ‘Strip Control’ bit in the controller’s Output Stream Control Register to initiate a specific stream (Stream ‘A’ in Figure 9) to be transmitted on multiple SDOs. In this case, the MSB of stream data is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a stripped stream. The codec does not support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not stripped. It is always transmitted on SDO0, and copied on SDO1.



**Figure 9. Stripped Stream on Multiple SDO**

### 7.2.3. Inbound Frame – Single SDI

An Inbound Frame – A single SDI is composed of one 36-Bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), the SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 10).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-Bit stream tag, one 6-Bit data length, and n-Bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 11).

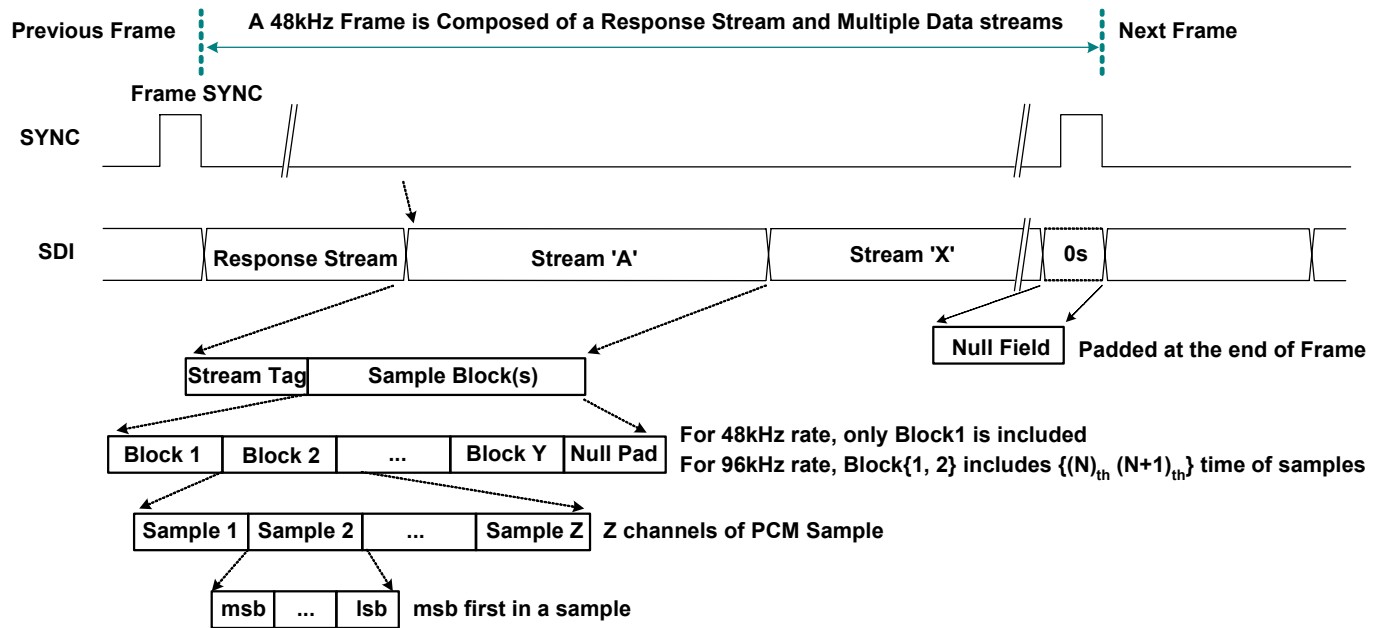


Figure 10. SDI Inbound Stream

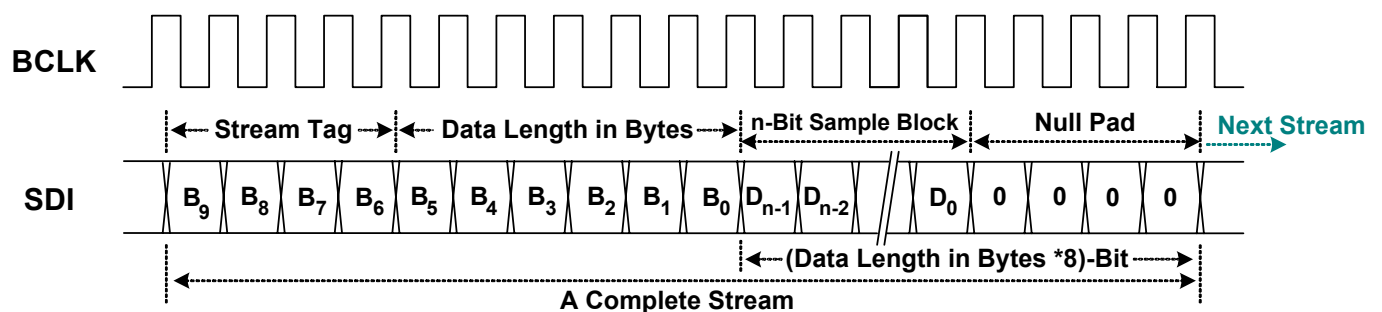
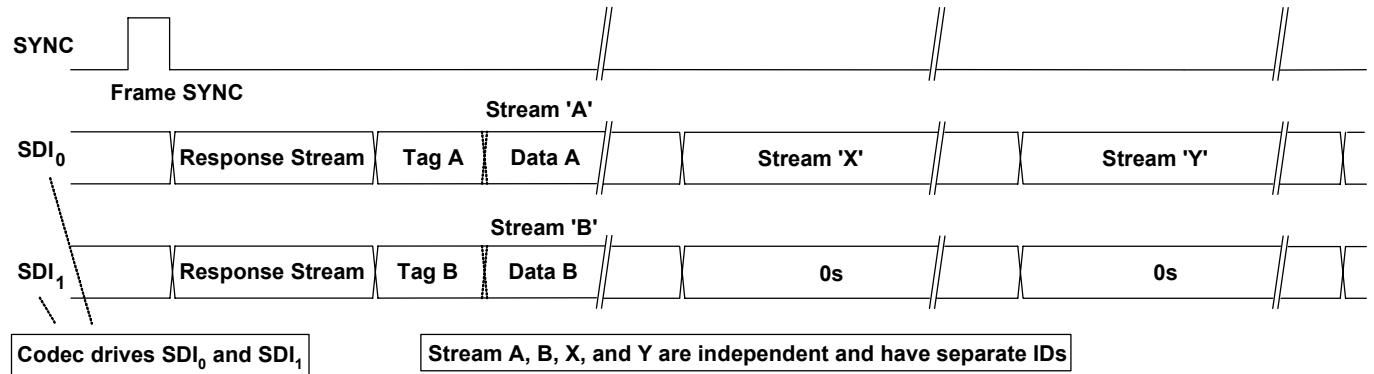


Figure 11. SDI Stream Tag and Data

### 7.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data into separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.



**Figure 12. Codec Transmits Data Over Multiple SDIs**

### 7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable sample rates are delivered in multiples or sub-multiples rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 7, page 16, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaved with n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 8, page 16, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames. The cadence

“12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)”

interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 9, page 17).

**Table 7. Defined Sample Rate and Transmission Rate**

| (Sub) Multiple | 48kHz Base                             | 44.1kHz Base                              |
|----------------|----------------------------------------|-------------------------------------------|
| 1/6            | 8kHz (1 sample block every 6 frames)   |                                           |
| 1/4            | 12kHz (1 sample block every 4 frames)  | 11.025kHz (1 sample block every 4 frames) |
| 1/3            | 16kHz (1 sample block every 3 frames)  |                                           |
| 1/2            |                                        | 22.05kHz (1 sample block every 2 frames)  |
| 2/3            | 32kHz (2 sample blocks every 3 frames) |                                           |
| 1              | 48kHz (1 sample block per frame)       | 44.1kHz (1 sample block per frame)        |
| 2              | 96kHz (2 sample blocks per frame)      | 88.2kHz (2 sample blocks per frame)       |
| 4              | 192kHz (4 sample blocks per frame)     | 176.4kHz (4 sample blocks per frame)      |

**Table 8. 48kHz Variable Rate of Delivery Timing**

| Rate   | Delivery Cadence           | Description                                       |
|--------|----------------------------|---------------------------------------------------|
| 8kHz   | YNNNNN (repeat)            | One sample block is transmitted in every 6 frames |
| 12kHz  | YNNN (repeat)              | One sample block is transmitted in every 4 frames |
| 16kHz  | YNN (repeat)               | One sample block is transmitted in every 3 frames |
| 32kHz  | Y <sup>2</sup> NN (repeat) | One sample block is transmitted in every 6 frames |
| 48kHz  | Y (repeat)                 | One sample block is transmitted in every 6 frames |
| 96kHz  | Y <sup>2</sup> (repeat)    | Two sample blocks are transmitted in each frame   |
| 192kHz | Y <sup>4</sup> (repeat)    | Four sample blocks are transmitted in each frame  |

*N: No sample block in a frame*

*Y: One sample block in a frame*

*Y<sup>x</sup>: X sample blocks in a frame*

| <b>Rate</b> | <b>Delivery Cadence</b>                                                                                                                                                                                                                |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11.025kHz   | {12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-} (repeat)                                                      |
| 22.05kHz    | {12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-} (repeat)                                                      |
| 44.1kHz     | 12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)                                                                                                                                                                                       |
| 88.2kHz     | 12 <sup>2</sup> -11 <sup>2</sup> -11 <sup>2</sup> -12 <sup>2</sup> -11 <sup>2</sup> -11 <sup>2</sup> -12 <sup>2</sup> -11 <sup>2</sup> -11 <sup>2</sup> -12 <sup>2</sup> -11 <sup>2</sup> -11 <sup>2</sup> -11 <sup>2</sup> - (repeat) |
| 174.4kHz    | 12 <sup>4</sup> -11 <sup>4</sup> -11 <sup>4</sup> -12 <sup>4</sup> -11 <sup>4</sup> -11 <sup>4</sup> -12 <sup>4</sup> -11 <sup>4</sup> -11 <sup>4</sup> -12 <sup>4</sup> -11 <sup>4</sup> -11 <sup>4</sup> -11 <sup>4</sup> - (repeat) |

$$\{ - \} = \text{NNNN}$$
$$\{11\} = \text{YNYNYNYNYNYNYNYNYNYNY}$$
$$\{ - \} = \mathbb{N} \mathbb{N}$$

|         |                                                                                                                      |
|---------|----------------------------------------------------------------------------------------------------------------------|
| 88.2kHz | 12 <sup>2</sup> - =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block. |
|---------|----------------------------------------------------------------------------------------------------------------------|

|          |                                                                                                                      |
|----------|----------------------------------------------------------------------------------------------------------------------|
| 174.4kHz | 12 <sup>4</sup> - =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block. |
|----------|----------------------------------------------------------------------------------------------------------------------|

### ***7.3. Reset and Initialization***

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset
2. Codec Reset
3. Codec changes its power state (for example, hot docking a codec to an HDA system)

#### **7.3.1. Link Reset**

A link reset may be caused by 3 events:

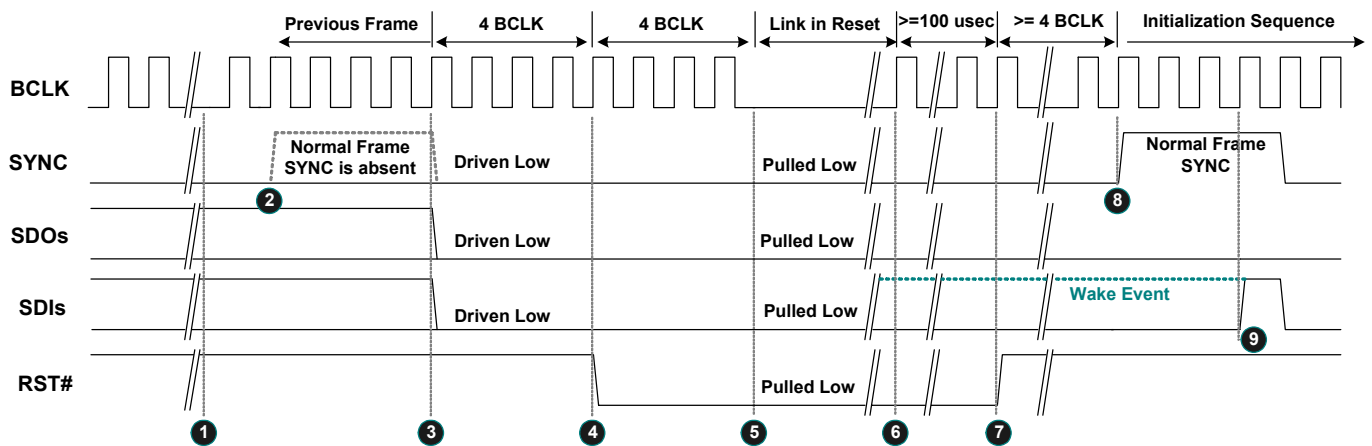
1. The HDA controller asserts RST# for any reason (power up, or PCI reset)
2. Software initiates a link reset via the 'CRST' bit in the Global Control Register (GCR) of the HDA controller
3. Software initiates power management sequences. Figure 13, page 19, shows the 'Link Reset' timing including the 'Enter' sequence (❶~❺) and 'Exit' sequence (❻~❾)

Enter 'Link Reset':

- ❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset
- ❷ As the controller completes the current frame, it does not signal the normal 8-Bit frame SYNC at the end of the frame
- ❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low
- ❹ The controller asserts the RST# signal to low, and enters the 'Link Reset' state
- ❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from ‘Link Reset’:

- ⑥ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)
- ⑦ Software is responsible for de-asserting RST# after a minimum of 100μs BCLK running time (the 100μsec provides time for the codec PLL to stabilize)
- ⑧ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC
- ⑨ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)



**Figure 13. Link Reset Timing**

### 7.3.2. Codec Reset

A ‘Codec Reset’ is initiated via the codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

### 7.3.3. Codec Initialization Sequence

- ❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller
- ❷ The codec will stop driving the SDI during this turnaround period
- ❸❹❺❻ The controller drives SDI to assign a CAD to the codec
- ❼ The controller releases the SDI after the CAD has been assigned
- ❽ Normal operation state

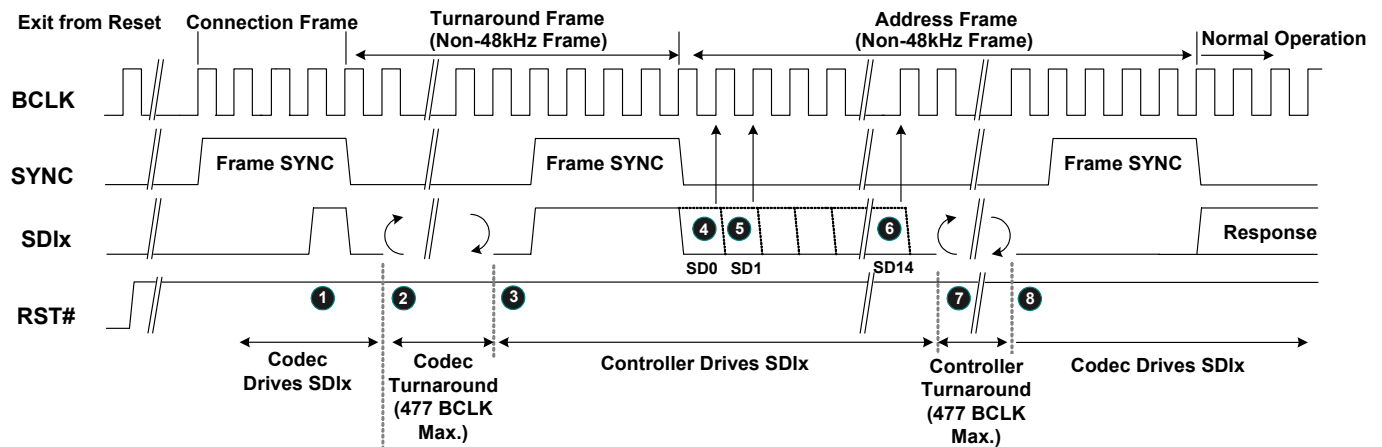


Figure 14. Codec Initialization Sequence

## 7.4. Verb and Response Format

### 7.4.1. Command Verb Format

There are two types of verbs: one with 4-Bit identifiers (4-Bit verbs) and 16-Bits of data, the other with 12-Bit identifiers (12-Bit verbs) and 8-Bits of data. Table 10 shows the 4-Bit verb structure of a command stream sent from the controller to operate the codec. Table 11 is the 12-Bit verb structure that gets and controls parameters in the codec.

Table 10. 40-Bit Commands in 4-Bit Verb Format

| Bit [39:32] | Bit [31:28]   | Bit [27:20] | Bit [19:16] | Bit [15:0] |
|-------------|---------------|-------------|-------------|------------|
| Reserved    | Codec Address | Node ID     | Verb ID     | Payload    |

Table 11. 40-Bit Commands in 12-Bit Verb Format

| Bit [39:32] | Bit [31:28]   | Bit [27:20] | Bit [19:8] | Bit [7:0] |
|-------------|---------------|-------------|------------|-----------|
| Reserved    | Codec Address | Node ID     | Verb ID    | Payload   |

## 7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-Bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The 'Tag' in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

**Table 12. Solicited Response Format**

| Bit [35] | Bit [34] | Bit [33:32] | Bit [31:0] |
|----------|----------|-------------|------------|
| Valid    | Unsol=0  | Reserved    | Response   |

**Table 13. Unsolicited Response Format**

| Bit [35] | Bit [34] | Bit [33:32] | Bit [31:28] | Bit [27:0] |
|----------|----------|-------------|-------------|------------|
| Valid    | Unsol=1  | Reserved    | Tag         | Response   |

*Note: The response stream in the link protocol is 36-Bits wide. The response is placed in the lower 32-bit field. Bit-35 is a 'Valid' bit to indicate the response is 'Ready'. Bit-34 is set to indicate that an unsolicited response was sent.*

## 7.5. Power Management

The ALC883 series does not support Wake-Up events when in low power mode. All power management state changes in widgets are driven by software. Table 14 shows the System Power State Definitions.

In the ALC883 series, all the widgets, including output/input converters, support power control. Software may have various power states depending on system configuration. Table 15 indicates those nodes that support power management. To simplify power control, software can configure whole codec power states through the audio function (NID=01h). Output converters (DACs) and input converters (ADCs) have no individual power control to supply fine-grained power control.

**Table 14. System Power State Definitions**

| Power States | Definitions                                                                                                                               |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| D0           | All power on. Individual DACs and ADCs can be powered up or down as required                                                              |
| D1           | All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up                               |
| D2           | All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference is off (D1 + analog reference off) |
| D3 (Hot)     | Power still supplied. The codec stops the internal clock. State is maintained                                                             |
| D3 (Cold)    | All power removed. State lost                                                                                                             |

**Table 15. Power Controls in NID 01h**

| Item                        | Description           | D0     | D1     | D2     | D3 | Link Reset |
|-----------------------------|-----------------------|--------|--------|--------|----|------------|
| Audio Function<br>(NID=01h) | LINK Response         | Normal | Normal | Normal | PD | PD         |
|                             | Front DAC             | Normal | PD     | PD     | PD | PD         |
|                             | Surr DAC)             | Normal | PD     | PD     | PD | PD         |
|                             | Cen/Lfe DAC           | Normal | PD     | PD     | PD | PD         |
|                             | Side DAC              | Normal | PD     | PD     | PD | PD         |
|                             | Fout DAC              | Normal | PD     | PD     | PD | PD         |
|                             | LINE ADC              | Normal | PD     | PD     | PD | PD         |
|                             | MIX ADC               | Normal | PD     | PD     | PD | PD         |
|                             | All Headphone Drivers | Normal | Normal | PD     | PD | Normal     |
|                             | All Mixers            | Normal | Normal | PD     | PD | Normal     |
|                             | All Reference         | Normal | Normal | PD     | PD | Normal     |

Note: PD=Powered Down

**Table 16. Powered Down Conditions**

| Condition                     | Description                                                                                                                                                                                                                                                      |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LINK Response powered down    | Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. S/PDIF-IN is also floated. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied |
| Front DAC powered down        | Analog block and digital filter are powered down                                                                                                                                                                                                                 |
| Surr DAC powered down         | Analog block and digital filter are powered down                                                                                                                                                                                                                 |
| CEN/LFE DAC powered down      | Analog block and digital filter are powered down                                                                                                                                                                                                                 |
| SIDESURR DAC powered down     | Analog block and digital filter are powered down                                                                                                                                                                                                                 |
| Fout DAC powered down         | Analog block and digital filter are powered down                                                                                                                                                                                                                 |
| LINE ADC powered down         | Analog block and digital filter are powered down. Data on SDATA-IN is quiet                                                                                                                                                                                      |
| MIX ADC powered down          | Analog block and digital filter are powered down. Data on SDATA-IN is quiet                                                                                                                                                                                      |
| Headphone Driver powered down | All headphone drivers are powered down                                                                                                                                                                                                                           |
| Mixers powered down           | All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complexes are still alive                                                                                                                                           |
| Reference power down          | All internal references, DC reference, and VREFOUTx at individual pin complexes are off                                                                                                                                                                          |

## 8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC883 series. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

### 8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. There are a total of 15 ID parameters defined for each widget, some parameters are supported only in a specific widget. Refer to section 7.4.1 Command Verb Format, page 20, to get detailed information about supported parameters.

**Table 17. Verb – Get Parameters (Verb ID=F00h)**

Get Parameter Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=00h | Verb ID=F00h | Parameter ID[7:0] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

*Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.*

#### 8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

**Table 18. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)**

Codec Response Format

| Bit   | Description                               |
|-------|-------------------------------------------|
| 31:16 | Vendor ID=10ECh (Realtek's PCI vendor ID) |
| 15:0  | Device ID=0883h                           |

*Note: The Root Node (NID=00h) supports this parameter.*

#### 8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

**Table 19. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)**

Codec Response Format

| Bit   | Description                                                                                                             |
|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Reserved. Read as 0's                                                                                                   |
| 23:20 | MajRev. The major version number (in decimal) of the HDA Spec to which the ALC883 series is fully compliant             |
| 19:16 | MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC883 series is fully compliant             |
| 15:8  | Revision ID. The vendor's revision number.<br>00h is for the first silicon version, 01h is for the second version, etc. |
| 7:0   | Stepping ID. The vendor's stepping number within the given Revision ID                                                  |

*Note: The Root Node (NID=00h in the ALC883 series) supports this parameter.*

### 8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node.

For function group nodes, it provides the total number of widgets associated with this function node.

**Table 20. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)**

Codec Response Format

| Bit   | Description                                                                                                                                                                    |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Reserved. Read as 0's                                                                                                                                                          |
| 23:16 | Starting Node Number<br>The starting node number in the sequential widgets                                                                                                     |
| 15:8  | Reserved. Read as 0's                                                                                                                                                          |
| 7:0   | Total Number of Nodes<br>For a root node, the total number of function groups in the root node<br>For a function group, the total number of widget nodes in the function group |

### 8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

**Table 21. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)**

Codec Response Format

| Bit  | Description                                                                                                                                 |
|------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved. Read as 0's                                                                                                                       |
| 7:0  | Function Group Type<br>00h: Reserved<br>01h: Audio Function<br>02h: Modem Function<br>03h~7Fh: Reserved<br>80h~FFh: Vendor Defined Function |

*Note: The Audio Function Group (NID=01h) supports this parameter.*

### 8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

**Table 22. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)**

Codec Response Format

| Bit   | Description                                                                                                    |
|-------|----------------------------------------------------------------------------------------------------------------|
| 31:17 | Reserved. Read as 0's                                                                                          |
| 16    | Beep Generator<br>A '1' indicates the presence of an integrated Beep generator within the Audio Function Group |
| 15:12 | Reserved. Read as 0's                                                                                          |
| 11:8  | Input Delay                                                                                                    |
| 7:4   | Reserved. Read as 0's                                                                                          |
| 3:0   | Output Delay                                                                                                   |

*Note: The Audio Function Group (NID=01h) supports this parameter.*

### 8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

**Table 23. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)**

Codec Response Format

| Bit   | Description                                                                                                                                                                                            |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Reserved. Read as 0's                                                                                                                                                                                  |
| 23:20 | Widget Type<br>0h: Audio Output    1h: Audio Input    2h: Mixer    3h: Selector    4h: Pin Complex<br>5h: Power Widget    6h: Volume Knob Widget    7h~Eh: Reserved    Fh: Vendor defined audio widget |
| 19:16 | Delay. Samples delayed between the HDA link and widgets                                                                                                                                                |
| 15:11 | Reserved. Read as 0's                                                                                                                                                                                  |
| 10    | Power Control<br>0: Power state control is not supported on this widget<br>1: Power state is supported on this widget                                                                                  |
| 9     | Digital<br>0: An analog input or output converter<br>1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)                                                     |
| 8     | ConnList. Connection List<br>0: Connected to HDA link. No Connection List Entry should be queried<br>1: Connection List Entry must be queried                                                          |
| 7     | UnsolCap. Unsolicited Capable<br>0: Unsolicited response is not supported<br>1: Unsolicited response is supported                                                                                      |
| 6     | ProcWidget. Processing Widget<br>0: No processing control<br>1: Processing control is supported                                                                                                        |
| 5     | Reserved. Read as 0                                                                                                                                                                                    |
| 4     | Format Override                                                                                                                                                                                        |
| 3     | AmpParOvr, AMP Param Override                                                                                                                                                                          |

**Codec Response Format**

| Bit | Description                                  |
|-----|----------------------------------------------|
| 2   | OutAmpPre. Out AMP Present                   |
| 1   | InAmpPre. In AMP Present                     |
| 0   | Stereo<br>0: Mono Widget<br>1: Stereo Widget |

### 8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameter in audio function provides default information about formats. Individual converters have their own parameters to provide supported formats if their ‘Format Override’ bit is set.

**Table 24. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)**
**Codec Response Format**

| Bit   | Description                                                                 |
|-------|-----------------------------------------------------------------------------|
| 31:21 | Reserved. Read as 0's                                                       |
| 20    | B32. 32-Bit audio format support<br>0: Not supported<br>1: Supported        |
| 19    | B24. 24-bit audio format support<br>0: Not supported<br>1: Supported        |
| 18    | B20. 20-bit audio format support<br>0: Not supported<br>1: Supported        |
| 17    | B16. 16-bit audio format support<br>0: Not supported<br>1: Supported        |
| 16    | B8. 24-bit audio format support<br>0: Not supported<br>1: Supported         |
| 15:12 | Reserved. Read as 0's                                                       |
| 11    | R12. 384kHz (=8*48kHz) rate support<br>0: Not supported<br>1: Supported     |
| 10    | R11. 192kHz (=4*48kHz) rate support<br>0: Not supported<br>1: Supported     |
| 9     | R10. 176.4kHz (=4*44.1kHz) rate support<br>0: Not supported<br>1: Supported |
| 8     | R9. 96kHz (=2*48kHz) rate support<br>0: Not supported<br>1: Supported       |

**Codec Response Format**

| Bit | Description                                                                                     |
|-----|-------------------------------------------------------------------------------------------------|
| 7   | R8. 88.2kHz ( $=2 \times 44.1\text{kHz}$ ) rate support<br>0: Not supported<br>1: Supported     |
| 6   | R7. 48kHz rate support<br>0: Not supported<br>1: Supported                                      |
| 5   | R6. 44.1kHz rate support<br>0: Not supported<br>1: Supported                                    |
| 4   | R5. 32kHz ( $=2/3 \times 48\text{kHz}$ ) rate support<br>0: Not supported<br>1: Supported       |
| 3   | R4. 22.05kHz ( $=1/2 \times 44.1\text{kHz}$ ) rate support<br>0: Not supported<br>1: Supported  |
| 2   | R3. 16kHz ( $=1/3 \times 48\text{kHz}$ ) rate support<br>0: Not supported<br>1: Supported       |
| 1   | R2. 11.025kHz ( $=1/4 \times 44.1\text{kHz}$ ) rate support<br>0: Not supported<br>1: Supported |
| 0   | R1. 8kHz ( $=1/6 \times 48\text{kHz}$ ) rate support<br>0: Not supported<br>1: Supported        |

### 8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the ‘Format Override’ bit is set.

**Table 25. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)**
**Codec Response Format**

| Bit  | Description                                 |
|------|---------------------------------------------|
| 31:3 | Reserved. Read as 0's                       |
| 2    | AC3<br>0: Not supported<br>1: Supported     |
| 1    | Float32<br>0: Not supported<br>1: Supported |
| 0    | PCM<br>0: Not supported<br>1: Supported     |

*Note: Input converters and output converters support this parameter.*

### 8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

**Table 26. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)**

Codec Response Format

| Bit      | Description                                                                                                                                                                                                  |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----------|--------|-----|------|---|---|----------|------|-----|----------|--------|-----|------|
| 31:16    | Reserved. Read as 0's                                                                                                                                                                                        |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 15:8     | VREF Control Capability<br>'1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD.                                                               |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
|          | <table><tr><td>7:6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Reserved</td><td>100%</td><td>80%</td><td>Reserved</td><td>Ground</td><td>50%</td><td>Hi-Z</td></tr></table> | 7:6 | 5        | 4      | 3   | 2    | 1 | 0 | Reserved | 100% | 80% | Reserved | Ground | 50% | Hi-Z |
|          | 7:6                                                                                                                                                                                                          | 5   | 4        | 3      | 2   | 1    | 0 |   |          |      |     |          |        |     |      |
| Reserved | 100%                                                                                                                                                                                                         | 80% | Reserved | Ground | 50% | Hi-Z |   |   |          |      |     |          |        |     |      |
|          |                                                                                                                                                                                                              |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 7        | L-R Swap. Indicates the capability of swapping the left and rights                                                                                                                                           |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 6        | Balanced I/O Pin<br>'1' indicates this pin complex has balanced pins                                                                                                                                         |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 5        | Input Capable<br>'1' indicates this pin complex supports input                                                                                                                                               |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 4        | Output Capable<br>'1' indicates this pin complex supports output                                                                                                                                             |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 3        | Headphone Drive Capable<br>'1' indicates this pin complex has an amplifier to drive a headphone                                                                                                              |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 2        | Presence Detect Capable<br>'1' indicates this pin complex can detect whether there is anything plugged in                                                                                                    |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 1        | Trigger Required<br>'1' indicates whether a software trigger is required for an impedance measurement                                                                                                        |     |          |        |     |      |   |   |          |      |     |          |        |     |      |
| 0        | Impedance Sense Capable<br>'1' indicates this pin complex can perform analog sense on the attached device to determine its type                                                                              |     |          |        |     |      |   |   |          |      |     |          |        |     |      |

*Note: Only Pin Complex widgets support this parameter.*

### 8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

**Table 27. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)**  
Codec Response Format

| Bit   | Description                                                                                                                                                                        |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | (Input) Mute Capable                                                                                                                                                               |
| 30:23 | Reserved. Read as 0                                                                                                                                                                |
| 22:16 | Step Size<br>Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB |
| 15    | Reserved. Read as 0                                                                                                                                                                |
| 14:8  | Number of Steps<br>Indicates the number of steps in the gain range. ‘0’ means the gain is fixed                                                                                    |
| 7     | Reserved. Read as 0                                                                                                                                                                |
| 6:0   | Offset<br>Indicates which step is 0dB                                                                                                                                              |

### 8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the ‘AMP Param Override’ bit is set.

**Table 28. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)**  
Codec Response Format

| Bit   | Description                                                                                                                                                                        |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | (Output) Mute Capable                                                                                                                                                              |
| 30:23 | Reserved. Read as 0                                                                                                                                                                |
| 22:16 | Step Size<br>Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. ‘0’ indicates a step of 0.25dB. ‘127’ indicates a step of 32dB |
| 15    | Reserved. Read as 0                                                                                                                                                                |
| 14:8  | Number of Steps<br>Indicates the number of steps in the gain range. ‘0’ means the gain is fixed                                                                                    |
| 7     | Reserved. Read as 0                                                                                                                                                                |
| 6:0   | Offset<br>Indicates which step is 0dB                                                                                                                                              |

### 8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

**Table 29. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)**

Codec Response Format

| Bit  | Description                                                                                                                                                                                         |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved. Read as 0                                                                                                                                                                                 |
| 7    | Short Form<br>0: Short Form<br>1: Long Form                                                                                                                                                         |
| 6:0  | Connect List Length<br>Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (Not a MUX widget) |

### 8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

**Table 30. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)**

Codec Response Format

| Bit  | Description                             |
|------|-----------------------------------------|
| 31:4 | Reserved. Read as 0's                   |
| 3    | D3Sup<br>1: Power state D3 is supported |
| 2    | D2Sup<br>1: Power state D2 is supported |
| 1    | D1Sup<br>1: Power state D1 is supported |
| 0    | D0Sup<br>1: Power state D0 is supported |

### 8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

**Table 31. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)**

Codec Response Format

| Bit   | Description                                                                                                      |
|-------|------------------------------------------------------------------------------------------------------------------|
| 31:16 | Reserved. Read as 0's                                                                                            |
| 15:8  | NumCoeff. Number of Coefficient                                                                                  |
| 7:1   | Reserved. Read as 0's                                                                                            |
| 0     | Benign<br>0: Processing unit is not linear and time invariant<br>1: Processing unit is linear and time invariant |

### 8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

**Table 32. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)**

Codec Response Format

| Bit   | Description                                                           |
|-------|-----------------------------------------------------------------------|
| 31    | GPIWake=0<br>The ALC883 series does not support GPIO wake up function |
| 30    | GPIUnsol=1<br>The ALC883 series supports GPIO unsolicited response    |
| 29:24 | Reserved. Read as 0's                                                 |
| 23:16 | NumGPIOs=00h<br>No GPI pin is supported                               |
| 15:8  | NumGPOs=00h<br>No GPO pin is supported                                |
| 7:0   | NumGPIOs=02h<br>Two GPIO pins are supported                           |

### 8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

**Table 33. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)**

Codec Response Format for NID=21h (Volume Control Knob)

| Bit  | Description                                                                                                                         |
|------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved. Read as 0's                                                                                                               |
| 7    | Delta<br>0: Software cannot modify the Volume Control Knob volume<br>1: Software can write a base volume to the Volume Control Knob |
| 6:0  | NumSteps<br>The number of steps in the range of the Volume Control Knob                                                             |

*Note: In devices without volume knob support, the ALC883 will respond with 0s to this parameter.*

## 8.2. Verb – Get Connection Select Control (Verb ID=F01h)

**Table 34. Verb – Get Connection Select Control (Verb ID=F01h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F01h | 0's               |

Codec Response Format

| Response [31:0]               |
|-------------------------------|
| Bit[7:0] are Connection Index |

Codec Response for Analog Port-A/B/C/D/E/F/G/H

| Bit  | Description                                                                                                                                                                                                     |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | 0's                                                                                                                                                                                                             |
| 7:0  | Connection Index currently Set (Default value is 00h)<br>00h: Sum Widget NID=0Ch<br>01h: Sum Widget NID=0Dh<br>02h: Sum Widget NID=0Eh<br>03h: Sum Widget NID=0Fh<br>04h: Sum Widget NID=26h<br>Other: Reserved |

Codec Response for Digital Pin S/PDIF-OUT

| Bit  | Description                                                                                                                                    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | 0's                                                                                                                                            |
| 7:0  | Connection Index currently Set (Default value is 00h)<br>00h: Digital Converter (S/PDIF-OUT)<br>01h: Pin Widget (S/PDIF-IN)<br>Other: Reserved |

Codec Response for other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.3. Verb – Set Connection Select (Verb ID=701h)

**Table 35. Verb – Set Connection Select (Verb ID=701h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0]  |
|-------------|-------------|--------------|--------------------|
| CAd=X       | Node ID=Xh  | Verb ID=701h | Select Index [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

## 8.4. Verb – Get Connection List Entry (Verb ID=F02h)

**Table 36. Verb – Get Connection List Entry (Verb ID=F02h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0]     |
|-------------|-------------|--------------|-----------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F02h | Offset Index - N[7:0] |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID=08h (LINE ADC)

| Bit  | Description                                                                            |
|------|----------------------------------------------------------------------------------------|
| 31:8 | Connection List Entry (N+3), (N+2) and (N+1)<br>Returns 000000h                        |
| 7:0  | Connection List Entry (N)<br>Returns 23h (Sum Widget) for N=0~3<br>Returns 00h for N>3 |

Codec Response for NID=09h (MIX ADC)

| Bit  | Description                                                                            |
|------|----------------------------------------------------------------------------------------|
| 15:8 | Connection List Entry (N+3), (N+2) and (N+1)<br>Returns 000000h                        |
| 7:0  | Connection List Entry (N)<br>Returns 22h (Sum Widget) for N=0~3<br>Returns 00h for N>3 |

Codec Response for NID=0Ah (S/PDIF-IN Converter)

| Bit  | Description                                                                                      |
|------|--------------------------------------------------------------------------------------------------|
| 31:8 | Connection List Entry (N+3), (N+2) and (N+1)<br>Returns 000000h                                  |
| 7:0  | Connection List Entry (N)<br>Returns 1Fh (S/PDIF-IN Pin Widget) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID=0Bh (Mixer)**

| Bit   | Description                                                                                                                                                                                           |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N+3)<br>Returns 1Bh (Pin Complex – LINE2) for N=0~3<br>Returns 15h (Pin Complex-SURR) for N=4~7<br>Returns 00h for N>7                                                         |
| 23:16 | Connection List Entry (N+2)<br>Returns 1Ah (Pin Complex – LINE1) for N=0~3<br>Returns 14h (Pin Complex – FRONT) for N=4~7<br>Returns 00h for N>7                                                      |
| 15:8  | Connection List Entry (N+1)<br>Returns 19h (Pin Complex – MIC2) for N=0~3.<br>Returns 1Dh (Pin Complex – PCBEEP) for N=4~7<br>Returns 17h (Pin Complex – SIDESURR) for N=8~11<br>Returns 00h for N>11 |
| 7:0   | Connection List Entry (N)<br>Returns 18h (Pin Complex – MIC1) for N=0~3<br>Returns 1Ch (Pin Complex – CD) for N=4~7<br>Returns 16h (Pin Complex – CEN/LFE) for N=8~11<br>Returns 00h for N>11         |

**Codec Response for NID=0Ch (Front Sum)**

| Bit   | Description                                                                           |
|-------|---------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N)<br>Returns 00h                                              |
| 23:16 | Connection List Entry (N+2)<br>Returns 00h                                            |
| 15:8  | Connection List Entry (N+1)<br>Returns 0Bh (Mixer) for N=0~3<br>Returns 00h for N>3   |
| 7:0   | Connection List Entry (N)<br>Returns 02h (Front DAC) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID=0Dh (Surround Sum)**

| Bit   | Description                                                                         |
|-------|-------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N)<br>Returns 00h                                            |
| 23:16 | Connection List Entry (N+2)<br>Returns 00h                                          |
| 15:8  | Connection List Entry (N+1)<br>Returns 0Bh (Mixer) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID=0Dh (Surround Sum)**

| Bit | Description                                                                                |
|-----|--------------------------------------------------------------------------------------------|
| 7:0 | Connection List Entry (N)<br>Returns 03h (Surround DAC) for N=0~3.<br>Returns 00h for N>3. |

**Codec Response for NID=0Eh (Cen/Lfe Sum)**

| Bit   | Description                                                                             |
|-------|-----------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N)<br>Returns 00h                                                |
| 23:16 | Connection List Entry (N+2)<br>Returns 00h                                              |
| 15:8  | Connection List Entry (N+1)<br>Returns 0Bh (Mixer) for N=0~3<br>Returns 00h for N>3     |
| 7:0   | Connection List Entry (N)<br>Returns 04h (Cen/Lfe DAC) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID=0Fh (Side-Surr Sum)**

| Bit   | Description                                                                           |
|-------|---------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N)<br>Returns 00h                                              |
| 23:16 | Connection List Entry (N+2)<br>Returns 00h                                            |
| 15:8  | Connection List Entry (N+1)<br>Returns 0Bh (Mixer) for N=0~3<br>Returns 00h for N>3   |
| 7:0   | Connection List Entry (N)<br>Returns 05h (Front DAC) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID=26h (Fout Sum)**

| Bit   | Description                                                                         |
|-------|-------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N)<br>Returns 00h                                            |
| 23:16 | Connection List Entry (N+2)<br>Returns 00h                                          |
| 15:8  | Connection List Entry (N+1)<br>Returns 0Bh (Mixer) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID=26h (Fout Sum)**

| Bit | Description                                                                           |
|-----|---------------------------------------------------------------------------------------|
| 7:0 | Connection List Entry (N)<br>Returns 25h (Fout1 DAC) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID=14h~1Bh (Port-A to port-H)**

| Bit   | Description                                                                                                                                  |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N+3)<br>Returns 0Fh (Sum Widget NID=0Fh) for N=0~3<br>Returns 00h for n>3                                             |
| 23:16 | Connection List Entry (N+2)<br>Returns 0Eh (Sum Widget NID=0Eh) for N=0~3<br>Returns 00h for N>3                                             |
| 15:8  | Connection List Entry (N+1)<br>Returns 0Dh (Sum Widget NID=0Dh) for N=0~3<br>Returns 00h for N>3                                             |
| 7:0   | Connection List Entry (N)<br>Returns 0Ch (Sum Widget NID=0Ch) for N=0~3<br>Returns 26h (Sum Widget NID=26h) for N=4~7<br>Returns 00h for N>7 |

**Codec Response for NID=1Eh (Pin Widget: S/PDIF-OUT)**

| Bit   | Description                                                                                      |
|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | Connection List Entry (N+3) and (N+2)<br>Returns 0000h                                           |
| 15:8  | Connection List Entry (N+1)<br>Returns 00h                                                       |
| 7:0   | Connection List Entry (N)<br>Returns 06h (S/PDIF-OUT converter) for N=0~3<br>Returns 00h for N>3 |

**Codec Response for NID= 22h/23h/ (Sum Widget before MIX/LINE ADCs)**

| Bit   | Description                                                                                                                                                                              |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Connection List Entry (N+3)<br>Returns 1Bh (Pin Complex – LINE2) for N=0~3<br>Returns 15h (Pin Complex-SURR) for N=4~7<br>Returns 00h for N>7                                            |
| 23:16 | Connection List Entry (N+2)<br>Returns 1Ah (Pin Complex – LINE1) for N=0~3<br>Returns 14h (Pin Complex – FRONT) for N=4~7<br>Returns 0Bh (Sum Widget) for N=8~11<br>Returns 00h for N>11 |

Codec Response for NID= 22h/23h/ (Sum Widget before MIX/LINE ADCs)

| Bit  | Description                                                                                                                                                                                          |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | Connection List Entry (N+1)<br>Returns 19h (Pin Complex – MIC2) for N=0~3<br>Returns 1Dh (Pin Complex – PCBEEP) for N=4~7<br>Returns 17h (Pin Complex – SIDESURR) for N=8~11<br>Returns 00h for N>11 |
| 7:0  | Connection List Entry (N)<br>Returns 18h (Pin Complex – MIC1) for N=0~3<br>Returns 1Ch (Pin Complex – CD) for N=4~7<br>Returns 16h (Pin Complex – CEN/LFE) for N=8~11<br>Returns 00h for N>11        |

Codec Response for Other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.5. Verb – Get Processing State (Verb ID=F03h)

**Table 37. Verb – Get Processing State (Verb ID=F03h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F03h | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit response |

Codec Response for All NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.6. Verb – Set Processing State (Verb ID=703h)

**Table 38. Verb – Set Processing State (Verb ID=703h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0]      |
|-------------|-------------|--------------|------------------------|
| CAd=X       | Node ID=Xh  | Verb ID=703h | Processing State [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

Codec Response for All NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

## 8.7. Verb – Get Coefficient Index (Verb ID=Dh)

**Table 39. Verb – Get Coefficient Index (Verb ID=Dh)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X       | Node ID=Xh  | Verb ID=Dh  | 0's                |

Codec Response Format

| Response [31:0]                  |
|----------------------------------|
| Bit [15:0] are Coefficient Index |

Codec Response for NID=20h (Realtek Define Registers)

| Bit   | Description           |
|-------|-----------------------|
| 31:16 | Reserved. Read as 0's |
| 15:0  | Coefficient Index     |

Codec Response for Other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.8. Verb – Set Coefficient Index (Verb ID=5h)

**Table 40. Verb – Set Coefficient Index (Verb ID=5h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0]       |
|-------------|-------------|-------------|--------------------------|
| CAd=X       | Node ID=Xh  | Verb ID=5h  | Coefficient Index [15:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

Codec Response for All NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

## 8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

**Table 41. Verb – Get Processing Coefficient (Verb ID=Ch)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X       | Node ID=Xh  | Verb ID=Ch  | 0's                |

Codec Response Format

| Response [31:0]               |
|-------------------------------|
| Processing Coefficient [15:0] |

Codec Response for NID=20h (Realtek Define Registers)

| Bit   | Description            |
|-------|------------------------|
| 31:16 | Reserved. Read as 0's  |
| 15:0  | Processing Coefficient |

Codec Response for Other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.10. Verb – Set Processing Coefficient (Verb ID=4h)

**Table 42. Verb – Set Processing Coefficient (Verb ID=4h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X       | Node ID=Xh  | Verb ID=4h  | Coefficient [15:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

Codec Response for All NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

## 8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

**Table 43. Verb – Get Amplifier Gain (Verb ID=Bh)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0]   |
|-------------|-------------|-------------|----------------------|
| CAd=X       | Node ID=Xh  | Verb ID=Bh  | ‘Get’ payload [15:0] |

Codec Response Format

| Response [31:0]                    |
|------------------------------------|
| Bit[7:0] are responsible for ‘Get’ |

‘Get’ Payload in Command Bit[15:0]

| Bit  | Description                                                                                                                              |
|------|------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | Get Input/Output<br>0: Input amplifier gain is requested<br>1: Output amplifier gain is requested                                        |
| 14   | Reserved. Read as 0.                                                                                                                     |
| 13   | Get Left/Right<br>0: Right amplifier gain is requested<br>1: Left amplifier gain is requested                                            |
| 12:4 | Reserved. Read as 0’s                                                                                                                    |
| 3:0  | Index[3:0] for Input Source<br>Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored |

Codec Response for 08h(LINE ADC) and 09h (MIX ADC)

| Bit  | Description                                                                                                                                                                                                                     |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | 0’s                                                                                                                                                                                                                             |
| 7    | Bit-15 is 0 in ‘Get Amplifier Gain’: Input Amplifier Mute, 0: Unmute, 1: Mute<br>Bit-15 is 1 in ‘Get Amplifier Gain’: Read as 0. (No Output Amplifier Mute)                                                                     |
| 6:0  | Bit-15 is 0 in ‘Get Amplifier Gain’: Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –16.5dB~+30dB in 1.5dB steps<br>Bit-15 is 1 in ‘Get Amplifier Gain’: Read as 0’s (No Output Amplifier Mute) |

Codec Response for NID=0Bh (MIXER Sum Widget)

| Bit  | Description                                                                                                                                                                                                                     |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | 0’s                                                                                                                                                                                                                             |
| 7    | Bit-15 is 0 in ‘Get Amplifier Gain’: Input Amplifier Mute. 0: Unmute 1: Mute (Default for all Index)<br>Bit-15 is 1 in ‘Get Amplifier Gain’: Read as 0. (No Output Amplifier Mute)                                              |
| 6:0  | Bit-15 is 0 in ‘Get Amplifier Gain’: Input Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from –34.5dB~+12dB in 1.5dB steps<br>Bit-15 is 1 in ‘Get Amplifier Gain’: Read as 0’s (No Output Amplifier Mute) |

Codec Response for NID=0Ch~0Fh (Sum Widget: Front, Surr, Cen/Lfe, SIDESURR Sum)

| Bit  | Description                                                                                                                                                                                                                  |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | 0's                                                                                                                                                                                                                          |
| 7    | Bit-15 is 0 in 'Get Amplifier Gain': Input Amplifier Mute, 0: Unmute, 1: Mute<br>Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute)                                                                   |
| 6:0  | Bit-15 is 0 in 'Get Amplifier Gain': Read as 0. (No Input Amplifier Gain)<br>Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Gain [6:0]. 7-bit step value (0~31) specifying the volume from -46.5dB~0dB in 1.5dB steps |

Codec Response for NID=14h~1Bh (Pin Complex: Front/Surr/CenLfe/SIDESURR/MIC1/MIC2/LINE1/LINE2)

| Bit  | Description                                                                                                                                               |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | 0's                                                                                                                                                       |
| 7    | Bit-15 is 0 in 'Get Amplifier Gain': Read as 0<br>Bit-15 is 1 in 'Get Amplifier Gain': Output Amplifier Mute, 0:Unmute, 1:Mute<br>(NID=14h~1Bh,Default=1) |
| 6:0  | Bit-15 is 0 in 'Get Amplifier Gain': Read as 0's<br>Bit-15 is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain)                             |

Codec Response to Other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

**Table 44. Verb – Set Amplifier Gain (Verb ID=3h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0]   |
|-------------|-------------|------------|---------------------|
| CAd=X       | Node ID=Xh  | Verb ID=3h | ‘Set’ payload [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0’s for all nodes |

‘Set’ Payload in Command Bit[15:0]

| Bit  | Description                                                                                                                                                                                                                                                                                               |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | Set Output Amp<br>1 indicates output amplifier gain will be set                                                                                                                                                                                                                                           |
| 14   | Set Input Amp<br>1 indicates input amplifier gain will be set                                                                                                                                                                                                                                             |
| 13   | Set Left Amp<br>1 indicates left amplifier gain will be set                                                                                                                                                                                                                                               |
| 12   | Set Right Amp<br>1 indicates right amplifier gain will be set                                                                                                                                                                                                                                             |
| 11:8 | Index Offset (for input amplifiers on Sum widgets and Selector Widgets)<br>5 bits index offset in connection list is used to select which input gain will be set on a Sum or a Selector widget. The index is ignored if the node is not a Sum or a Selector widget, or the ‘Set Input Amp’ bit is not set |
| 7    | Mute<br>0: Unmute<br>1: Mute ( $-\infty$ gain)                                                                                                                                                                                                                                                            |
| 6:0  | Gain[6:0]<br>A 7-bit step value specifying the amplifier gain                                                                                                                                                                                                                                             |

### 8.13. Verb – Get Converter Format (Verb ID=Ah)

**Table 45. Verb – Get Converter Format (Verb ID=Ah)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X       | Node ID=Xh  | Verb ID=Ah  | 0's                |

Codec Response Format

| Response [31:0]                |
|--------------------------------|
| Bit[15:0] are converter format |

Codec Response for NID=02h~06h, 25h (Output Converters: Front, Surr, Cen/Lfe, Side-Surr, Fout DAC, S/PDIF-OUT).

Codec Response for NID=08h~0Ah (Input Converters: LINE, MIX DAC, and S/PDIF-IN)

| Bit   | Description                                                                                                                                                                                       |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Reserved. Read as 0                                                                                                                                                                               |
| 15    | Stream Type (TYPE)<br>0: PCM<br>1: Non-PCM                                                                                                                                                        |
| 14    | Sample Base Rate (BASE)<br>0: 48kHz<br>1: 44.1kHz                                                                                                                                                 |
| 13:11 | Sample Base Rate Multiple (MULT)<br>000b: *1    001b: *2    010b: *3    011b: *4    100b~111b: Reserved                                                                                           |
| 10:8  | Sample Base Rate Divisor (DIV)<br>000b: /1    001b: /2    010b: /3    011b: /4    100b: /5    101b: /6    110b: /7    111b: /8<br>The ALC883 series does not support Divisor. Always read as 000b |
| 7     | Reserved. Read as 0.                                                                                                                                                                              |
| 6:4   | Bits per Sample (BITS)<br>000b: 8 bits    001b: 16 bits    010b: 20 bits    011b: 24 bits    100b: 32 bits    101b~111b: reserved                                                                 |
| 3:0   | Number of Channels<br>0: 1 channel    1: 2 channels    2: 3 channels    .....    15: 16 channels                                                                                                  |

Codec Response for other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.14. Verb – Set Converter Format (Verb ID=2h)

**Table 46. Verb – Set Converter Format (Verb ID=2h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:16] | Payload Bit [15:0] |
|-------------|-------------|-------------|--------------------|
| CAd=X       | Node ID=Xh  | Verb ID=2h  | Set format [15:0]  |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

‘Set’ Payload in Command Bit[15:0]

| Bit   | Description                                                                                                                                                                                       |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Reserved. Read as 0                                                                                                                                                                               |
| 15    | Stream Type (TYPE)<br>0: PCM<br>1: Non-PCM                                                                                                                                                        |
| 14    | Sample Base Rate (BASE)<br>0: 48kHz<br>1: 44.1kHz                                                                                                                                                 |
| 13:11 | Sample Base Rate Multiple (MULT)<br>000b: *1    001b: *2    010b: *3    011b: *4    100b~111b: Reserved                                                                                           |
| 10:8  | Sample Base Rate Divisor (DIV)<br>000b: /1    001b: /2    010b: /3    011b: /4    100b: /5    101b: /6    110b: /7    111b: /8<br>The ALC883 series does not support Divisor. Always read as 000b |
| 7     | Reserved. Read as 0                                                                                                                                                                               |
| 6:4   | Bits per Sample (BITS)<br>000b: 8 bits    001b: 16 bits    010b: 20 bits    011b: 24 bits    100b: 32 bits    101b~111b: Reserved                                                                 |
| 3:0   | Number of Channels<br>0: 1 channel    1: 2 channels    2: 3 channels    .....    15: 16 channels                                                                                                  |

## 8.15. Verb – Get Power State (Verb ID=F05h)

**Table 47. Verb – Get Power State (Verb ID=F05h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8] | Payload Bit [7:0] |
|-------------|-------------|------------|-------------------|
| CAd=X       | Node ID=01h | Verb ID=Ah | 0's               |

Codec Response Format

| Response [31:0]   |
|-------------------|
| Power State [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                                                                                                                                                        |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | Reserved. Read as 0's                                                                                                                                                                                                                                                              |
| 5:4  | PS-Act. Actual Power State [1:0]<br>00: Power state is D0<br>01: Power state is D1<br>10: Power state is D2<br>11: Power state is D3<br>PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set |
| 3:2  | Reserved. Read as 0's                                                                                                                                                                                                                                                              |
| 1:0  | PS-Set, Set Power State [1:0]<br>00: Power state is D0<br>01: Power state is D1<br>10: Power state is D2<br>11: Power state is D3<br>PS-Set controls the current power setting of the referenced node                                                                              |

Codec Response for other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.16. Verb – Set Power State (Verb ID=705h)

**Table 48. Verb – Set Power State (Verb ID=705h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=01h | Verb ID=705h | Power State [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

'Power State' in Command Bit[7:0]

| Bit | Description                                                                                                                                                                                             |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved. Read as 0's                                                                                                                                                                                   |
| 5:4 | PS-Act. Actual Power State [1:0]<br>00: Power state is D0<br>01: Power state is D1<br>10: Power state is D2<br>11: Power state is D3<br>PS-Act indicates the actual power state of the referenced node. |
| 3:2 | Reserved. Read as 0's                                                                                                                                                                                   |
| 1:0 | PS-Set. Set Power State [1:0]<br>00: Power state is D0<br>01: Power state is D1<br>10: Power state is D2<br>11: Power state is D3                                                                       |

## 8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

**Table 49. Verb – Get Converter Stream, Channel (Verb ID=F06h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F06h | 0's               |

Codec Response Format

| Response [31:0]        |
|------------------------|
| Stream & Channel [7:0] |

Codec Response for NID=02h~06h, 25h (Output Converters: Front, Surr, Cen/Lfe, Side-Surr, Fout DAC, S/PDIF-OUT)

Codec Response for NID=08h~0Ah (Input Converters: LINE ADC, MIX DAC, and S/PDIF-IN)

| Bit  | Description                                                                                                                                           |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved. Read as 0's                                                                                                                                 |
| 7:4  | Stream[3:0]<br>The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.                                                      |
| 3:0  | Channel[3:0]<br>The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel |

Codec Response for other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

**Table 49. Verb – Set Converter Stream, Channel (Verb ID=706h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0]      |
|-------------|-------------|--------------|------------------------|
| CAd=X       | Node ID=Xh  | Verb ID=706h | Stream & Channel [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

‘Stream and Channel’ in Command Bit[7:0]

| Bit  | Description                                                                                                                                               |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved. Read as 0's                                                                                                                                     |
| 7:4  | Set Stream[3:0]<br>The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.                                                      |
| 1:0  | Set Channel[3:0]<br>The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel |

*Note: This verb assigns stream and channel for output converters (NID=02h~06h, 25h) and input converters (NID=08h~0Ah). Other widgets will ignore this verb.*

## 8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

**Table 50. Verb – Get Pin Widget Control (Verb ID=F07h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F07h | 0's               |

Codec Response Format

| Response [31:0]   |
|-------------------|
| Pin Control [7:0] |

Codec Response for NID=14h~1Bh

(Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, and LINE2)

| Bit  | Description                                                                                   |
|------|-----------------------------------------------------------------------------------------------|
| 31:1 | Reserved. Read as 0's                                                                         |
| 7    | H-Phn Enable (Headphone Amplifier Enable, EN_AMP for a I/O unit)<br>0: Disabled<br>1: Enabled |
| 6    | Out Enable (Output Buffet Enable, EN_OBUF for a I/O unit)<br>0: Disabled<br>1: Enabled        |
| 5    | In Enable (Input Buffer Enable, EN_IBUF for a I/O unit)<br>0: Disabled<br>1: Enabled          |
| 4:   | Reserved                                                                                      |

Codec Response for NID=14h~1Bh

(Pin Complex: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, and LINE2)

| Bit | Description                                                                                                                                                                          |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | VrefEn (Vrefout Enable Control)<br>000b: Hi-Z (Disabled)<br>001b: 50% of AVDD<br>010b: Ground 0V<br>011b: Reserved<br>100b: 80% of AVDD<br>101b: 100% of AVDD<br>110b~111b: Reserved |

Codec Response for other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.20. Verb – Set Pin Widget Control (Verb ID=707h)

**Table 51. Verb – Set Pin Widget Control (Verb ID=707h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=707h | Pin Control [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

'Pin Control' in command [7:0]: (Pin: FRONT, SURR, CENLFE, SIDESURR, MIC1, MIC2, LINE1, and LINE2)

| Bit  | Description                                                                                                                                                                          |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | Reserved. Read as 0's                                                                                                                                                                |
| 7    | H-Phn Enable<br>0: Disabled<br>1: Enabled                                                                                                                                            |
| 6    | Out Enable<br>0: Disabled<br>1: Enabled                                                                                                                                              |
| 5    | In Enable (Input Buffer Enable, EN_IBUF for a I/O unit)<br>0: Disabled<br>1: Enabled                                                                                                 |
| 4:   | Reserved                                                                                                                                                                             |
| 2:0  | VrefEn (Vrefout Enable Control)<br>000b: Hi-Z (Disabled)<br>001b: 50% of AVDD<br>010b: Ground 0V<br>011b: Reserved<br>100b: 80% of AVDD<br>101b: 100% of AVDD<br>110b~111b: Reserved |

## 8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real-time event.

**Table 52. Verb – Get Unsolicited Response Control (Verb ID=F08h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]    | Payload Bit [7:0] |
|-------------|-------------|---------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID= F08h | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID=01h (GPIO), 0Ah (S/PDIF-IN), 14h~1Bh (Port)

| Bit  | Description                                                                                                                             |
|------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved. Read as 0's                                                                                                                   |
| 7    | Unsolicited Response is Enabled<br>0: Disabled<br>1: Enabled                                                                            |
| 6:4  | Reserved. Read as 0's                                                                                                                   |
| 3:0  | Assigned Tag for Unsolicited Response<br>The tag[3:0] is assigned by software to determine which widget generates unsolicited responses |

Codec Response for other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enable a widget to generate an unsolicited response.

**Table 53. Verb – Set Unsolicited Response Control (Verb ID=708h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=708h | EnableUnsol [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

'EnableUnsol' in Command Bit[7:0]

| Bit  | Description                                                                                                                                        |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved. Read as 0's                                                                                                                              |
| 7    | Enable Unsolicited Response<br>0: Disable<br>1: Enable                                                                                             |
| 6:4  | Reserved. Read as 0's                                                                                                                              |
| 3:0  | Tag for Unsolicited Response<br>Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses |

## 8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

**Table 54. Verb – Get Pin Sense (Verb ID=F09h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]    | Payload Bit [7:0] |
|-------------|-------------|---------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID= F09h | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID = 14h~1Bh, 1Eh, 1Fh

| Bit  | Description                                                                                            |
|------|--------------------------------------------------------------------------------------------------------|
| 31   | Presence Detect Status<br>0: No device is attached to the pin<br>1: Device is attached to the pin      |
| 30:0 | Measured Impedance<br>The ALC883 does not support hardware impedance detect. This field is read as 0s. |

Codec Response for other NID

| Bit  | Description                       |
|------|-----------------------------------|
| 31:0 | Not supported (returns 00000000h) |

## 8.24. Verb – Execute Pin Sense (Verb ID=709h)

**Table 55. Verb – Execute Pin Sense (Verb ID=709h)**

Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]    | Payload Bit [7:0] |
|-------------|-------------|---------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID= 709h | Right Channel[0]  |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

'Payload' in Command Bit[7:0]

| Bit | Description                                                                                 |
|-----|---------------------------------------------------------------------------------------------|
| 7:1 | Reserved. Read as 0's                                                                       |
| 0   | Right (Ring) Channel Select<br>0: Sense Left channel (Tip)<br>1: Sense Right channel (Ring) |

## 8.25. Verb – Get Configuration Default (Verb ID=F1Ch)

Reads the 32-bit sticky register for each Pin Widget configured by software.

**Table 56. Verb – Get Configuration Default (Verb ID=F1Ch)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]    | Payload Bit [7:0] |
|-------------|-------------|---------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID= F1Ch | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID=14h, 15h, 16h, 17h, 18h, 19h, 1Ah, 1Bh, 1Eh, and 1Fh

| Bit  | Description                                          |
|------|------------------------------------------------------|
| 31:0 | 32-bit configuration information for each pin widget |

*Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).*

## 8.26. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh such as placement and expected default device.

**Table 57. Verb – Set Configuration Default Bytes 0, 1, 2, 3  
(Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]                        | Payload Bit [7:0] |
|-------------|-------------|-----------------------------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=71Ch,<br>71Dh, 71Eh, 71Fh | Label [7:0]       |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

*Note: Supported by Pin Widget NID=14h~1Bh, 1Eh and 1Fh. Other widgets will ignore this verb.*

Codec Response for All NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

## 8.27. Verb – Get BEEP Generator (Verb ID=F0Ah)

**Table 58. Verb – Get BEEP Generator (Verb ID= F0Ah)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]    | Payload Bit [7:0] |
|-------------|-------------|---------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID= F1Bh | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| Divider [7:0]   |

‘Response’ for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                                                                                                                                                                                                  |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                                                                                                                                                                                                     |
| 7:0  | Frequency Divider, F[7:0]<br>The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]<br>The lowest tone is 48kHz/(255*4)=47Hz<br>The highest tone is 48kHz/(1*4)=12kHz<br>A value of 00h in F[7:0] disables internal BEEP generator and allows external PCBEEP input |

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

## 8.28. Verb – Set BEEP Generator (Verb ID=70Ah)

**Table 59. Verb – Set BEEP Generator (Verb ID= 70Ah)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=71Bh | Divider [7:0]     |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

‘Divider’ in Set Command

| Bit  | Description                                                                                                                                                                                                                                                                                                                      |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                                                                                                                                                                                                         |
| 7:0  | Frequency Divider, F[7:0]<br>The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]<br>The lowest tone is 48kHz/(255*4)=47Hz<br>The highest tone is 48kHz/(1*4)=12kHz<br>A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input |

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for All NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

## 8.29. Verb – Get GPIO Data (Verb ID= F15h)

**Table 60. Verb – Get GPIO Data (Verb ID= F15h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F15h | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| 32-bit Response |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                              |
|------|----------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                 |
| 7:2  | GPIO[7:2] Data. Not supported in the ALC883 series                                                       |
| 1:0  | GPIO[1:0] Data<br>The value written (output) or sensed (input) on the corresponding pin if it is enabled |

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

## 8.30. Verb – Set GPIO Data (Verb ID= 715h)

**Table 61. Verb – Set GPIO Data (Verb ID= 715h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=715h | Data [7:0]        |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

'Data' in Set command for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                         |
|------|---------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                            |
| 7:2  | GPIO[7:2] output Data. Not supported in the ALC883 series                                                           |
| 1:0  | GPIO[1:0] Output Data<br>The value written determines the value driven on a pin that is configured as an output pin |

Codec Response for All NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

### 8.31. Verb – Get GPIO Enable Mask (Verb ID=F16h)

**Table 62. Verb – Get GPIO Enable Mask (Verb ID= F16h)**

| Get Command Format |             |              |                   | Codec Response Format |  |
|--------------------|-------------|--------------|-------------------|-----------------------|--|
| Bit [31:28]        | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] | Response [31:0]       |  |
| CAd=X              | Node ID=Xh  | Verb ID=F16h | 0's               | EnableMask [7:0]      |  |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                                                                   |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                                                                      |
| 7:2  | Reserved                                                                                                                                                                                      |
| 1:0  | GPIO[1:0] Enable mask<br>0: The corresponding GPIO pin is disabled and is in Hi-Z state<br>1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control |

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

### 8.32. Verb – Set GPIO Enable Mask (Verb ID=716h)

**Table 63. Verb – Set GPIO Enable Mask (Verb ID=716h)**

| Set Command Format |             |              |                   | Codec Response Format |  |
|--------------------|-------------|--------------|-------------------|-----------------------|--|
| Bit [31:28]        | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] | Response [31:0]       |  |
| CAd=X              | Node ID=Xh  | Verb ID=716h | Enable Mask [7:0] | 0's for all nodes     |  |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                                                                   |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                                                                      |
| 7:2  | GPIO[7:2] Enable Mask. Not supported in the ALC883 series                                                                                                                                     |
| 1:0  | GPIO[1:0] Enable Mask<br>0: The corresponding GPIO pin is disabled and is in Hi-Z state<br>1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control |

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for All NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

### 8.33. Verb – Get GPIO Direction (Verb ID=F17h)

**Table 64. Verb – Get GPIO Direction (Verb ID=F17h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F17h | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| Direction [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                        |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                           |
| 7:2  | GPIO[7:2] Direction Control. Not supported in the ALC883 series                                                                                    |
| 1:0  | GPIO[1:0] Direction Control<br>0: The corresponding GPIO pin is configured as an input<br>1: The corresponding GPIO pin is configured as an output |

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

### 8.34. Verb – Set GPIO Direction (Verb ID=717h)

**Table 65. Verb – Set GPIO Direction (Verb ID=717h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=717h | Direction [7:0]   |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                        |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                           |
| 7:2  | GPIO[7:2] Direction Control. Not supported in the ALC883 series                                                                                    |
| 1:0  | GPIO[1:0] Direction Control<br>0: The corresponding GPIO pin is configured as an input<br>1: The corresponding GPIO pin is configured as an output |

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

### 8.35. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

**Table 66. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F19h | 0's               |

Codec Response Format

| Response [31:0]   |
|-------------------|
| UnsolEnable [7:0] |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                                                             |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                                                                |
| 7:2  | GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC883 series                                                                                                                   |
| 1:0  | GPIO[1:0] Unsolicited Enable mask<br>0: Unsolicited response will not be sent on link<br>1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed |

*Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.*

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

### 8.36. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

**Table 67. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)**

Set Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=719h | UnsolEnable [7:0] |

Codec Response Format

| Response [31:0]   |
|-------------------|
| 0's for all nodes |

Codec Response for NID=01h (Audio Function Group)

| Bit  | Description                                                                                                                                                                             |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                                                                |
| 7:2  | GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC883 series                                                                                                                   |
| 1:0  | GPIO[1:0] Unsolicited Enable Mask<br>0: Unsolicited response will not be sent on link<br>1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed |

*Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.*

*Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb- 'Unsolicited Response' for NID=01h are enabled.*

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0's         |

### 8.37. Verb – Function Reset (Verb ID=7FFh)

**Table 68. Verb – Function Reset (Verb ID=7FFh)**

Command Format (NID=01H)

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=01h | Verb ID=7FFh | 0's               |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's             |

Codec Response

| Bit  | Description           |
|------|-----------------------|
| 31:0 | Reserved. Read as 0's |

Note: The Function Reset command causes all widgets in the ALC883 series to return to their power on default state.

### 8.38. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)

**Table 69. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID= F0Dh, F0Eh)**

Get Command Format

| Bit [31:28] | Bit [27:20] | Bit [19:8]            | Payload Bit [7:0] |
|-------------|-------------|-----------------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=F0Dh/<br>F0Eh | 0's               |

Codec Response Format

| Response [31:0]                       |
|---------------------------------------|
| Bit[31:16]=0's, Bit[15:0] are SIC bit |

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Dh (Control 1 for SIC bit[15:0])

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Eh (Control 2 for SIC bit[15:0])

| Bit   | Description – SIC (S/PDIF IEC Control) Bit[7:0]                                       |
|-------|---------------------------------------------------------------------------------------|
| 31:16 | Read as 0's                                                                           |
| 15    | Reserved. Read as 0's                                                                 |
| 14:8  | CC[6:0] (Category Code)                                                               |
| 7     | LEVEL (Generation Level)                                                              |
| 6     | PRO (Professional or Consumer format)<br>0: Consumer format<br>1: Professional format |
| 5     | /AUDIO (Non-Audio Data type)<br>0: PCM data<br>1: AC3 or other digital non-audio data |
| 4     | COPY (Copyright)<br>0: Asserted<br>1: Not asserted                                    |
| 3     | PRE (Pre-emphasis)<br>0: None<br>1: Filter pre-emphasis is 50/15 microseconds         |
| 2     | VCFG for Validity Control (control V bit and data in Sub-Frame)                       |
| 1     | V for Validity Control (control V bit and data in Sub-Frame)                          |

NID=06h (S/PDIF-OUT) Response to ‘Get verb’ – F0Dh (Control 1 for SIC bit[15:0])

NID=06h (S/PDIF-OUT) Response to ‘Get verb’ – F0Eh (Control 2 for SIC bit[15:0])

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|-------------------------------------------------|
| 0   | Digital Enable. DigEn<br>0: OFF<br>1: ON        |

NID=0Ah (S/PDIF-IN) Response to ‘Get verb (F0Dh)

NID=0Ah (S/PDIF-IN) Response to ‘Get verb (F0Eh)

| Bit   | Description (part of S/PDIF-IN Channel Status)                                                                                                    |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Reserved. Read as 0’s                                                                                                                             |
| 15    | Reserved. Read as 0’s                                                                                                                             |
| 14:8  | CC[6:0] (Category Code)                                                                                                                           |
| 7     | LEVEL (Generation Level)                                                                                                                          |
| 6     | PRO (Professional or Consumer format)<br>0: Consumer format<br>1: Professional format                                                             |
| 5     | /AUDIO (Non-Audio Data type)<br>0: PCM data<br>1: AC3 or other digital non-audio data                                                             |
| 4     | COPY (Copyright)<br>0: Asserted<br>1: Not asserted                                                                                                |
| 3     | PRE (Pre-emphasis)<br>0: None<br>1: Filter pre-emphasis is 50/15 microseconds                                                                     |
| 2     | Reserved                                                                                                                                          |
| 1     | In‘V’alid. V bit in sub-frame of S/PDIF-IN<br>0: Data X and Y are valid, or S/PDIF-IN is not locked<br>1: At least one of data X and Y is invalid |
| 0     | Digital Enable. DigEn<br>0: OFF<br>1: ON                                                                                                          |

Codec Response for Other NID

| Bit  | Description |
|------|-------------|
| 31:0 | 0’s         |

## 8.39. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

**Table 70. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)**

Set Command Format (Verb ID=70Xh, Set Control 1)

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=70Dh | SIC [7:0]         |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's             |

Set Command Format (Verb ID=70Yh, Set Control 2)

| Bit [31:28] | Bit [27:20] | Bit [19:8]   | Payload Bit [7:0] |
|-------------|-------------|--------------|-------------------|
| CAd=X       | Node ID=Xh  | Verb ID=70Eh | SIC [15:8]        |

Codec Response Format

| Response [31:0] |
|-----------------|
| 0's             |

‘Payload’ in Set Control 1 for NID=06h (S/PDIF-OUT)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0]                                       |
|-----|---------------------------------------------------------------------------------------|
| 7   | LEVEL (Generation Level)                                                              |
| 6   | PRO (Professional or Consumer format)<br>0: Consumer format<br>1: Professional format |
| 5   | /AUDIO (Non-Audio Data type)<br>0: PCM data<br>1: AC3 or other digital non-audio data |
| 4   | COPY (Copyright)<br>0: Asserted<br>1: Not asserted                                    |
| 3   | PRE (Pre-emphasis)<br>0: None<br>1: Filter pre-emphasis is 50/15 microseconds         |
| 2   | VCFG for Validity Control (control V bit and data in Sub-Frame)                       |
| 1   | V for Validity Control (control V bit and data in Sub-Frame)                          |
| 0   | Digital Enable. DigEn<br>0: OFF<br>1: ON                                              |

‘Payload’ in Set Control 2 for NID=06h (S/PDIF-OUT)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|-------------------------------------------------|
| 7   | Reserved. Read as 0’s                           |
| 6:0 | CC[6:0] (Category Code)                         |

‘Payload’ in Set Control 1 for NID=0Ah (S/PDIF-IN)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|-------------------------------------------------|
| 7:1 | Reserved                                        |
| 0   | Digital Enable. DigEn<br>0: OFF<br>1: ON        |

‘Payload’ in Set Control 2 for NID=0Ah (S/PDIF-IN)

| Bit | Description – SIC (S/PDIF IEC Control) Bit[7:0] |
|-----|-------------------------------------------------|
| 7:0 | Reserved. Read as 0’s                           |

*Note: Other widgets will ignore this verb.*

## 9. Electrical Characteristics

### 9.1. DC Characteristics

#### 9.1.1. Absolute Maximum Ratings

**Table 71. Absolute Maximum Ratings**

| Parameter                     | Symbol | Minimum | Typical | Maximum | Units |
|-------------------------------|--------|---------|---------|---------|-------|
| Power Supply:                 |        |         |         |         |       |
| Digital                       | DVDD   | 3.0     | 3.3     | 3.6     | V     |
| Analog                        | AVDD*  | 3.5     | 5.0     | 5.25    | V     |
| Ambient Operating Temperature | Ta     | 0       | -       | +70     | °C    |
| Storage Temperature           | Ts     |         |         | +125    | °C    |

*Note\** The standard testing condition before shipping is AVDD = 5.0V unless specified. Customers designing with a different AVDD should contact Realtek technical support representatives for special testing support.

#### 9.1.2. Threshold Voltage

DVDD= 3.3V±5%, T<sub>ambient</sub>=25°C, with 50pF external load.

**Table 72. Threshold Voltage**

| Parameter                                                | Symbol          | Minimum              | Typical | Maximum             | Units |
|----------------------------------------------------------|-----------------|----------------------|---------|---------------------|-------|
| Input Voltage Range                                      | V <sub>in</sub> | -0.30                | -       | DVDD +0.30          | V     |
| Low Level Input Voltage<br>(BCLK, RST#, SDO, SYNC, SDI)  | V <sub>IL</sub> | -                    | -       | 0.30*DVDD<br>(1.00) | V     |
| High Level Input Voltage<br>(BCLK, RST#, SDO, SYNC, SDI) | V <sub>IH</sub> | 0.65* DVDD<br>(2.00) | -       | -                   | V     |
| Low Level Input Voltage<br>(S/PDIF-IN/OUT, GPIOs)        | V <sub>IL</sub> | -                    | -       | 0.44*DVDD<br>(1.45) | V     |
| High Level Input Voltage<br>(S/PDIF-IN/OUT, GPIOs)       | V <sub>IH</sub> | 0.56* DVDD<br>(1.85) | -       | -                   | V     |
| High Level Output Voltage                                | V <sub>OH</sub> | 0.9*DVDD             |         | -                   | V     |
| Low Level Output Voltage                                 | V <sub>OL</sub> | -                    | -       | 0.1*DVDD            | V     |
| Input Leakage Current                                    | -               | -10                  | -       | 10                  | μA    |
| Output Leakage Current (Hi-Z)                            | -               | -10                  | -       | 10                  | μA    |
| Output Buffer Drive Current                              | -               | -                    | 5       | -                   | mA    |
| Internal Pull Up Resistance                              | -               | -                    | 50k     | -                   | Ω     |

### 9.1.3. Digital Filter Characteristics

**Table 73. Digital Filter Characteristics**

| Filter             | Symbol                      | Minimum | Typical | Maximum | Units |
|--------------------|-----------------------------|---------|---------|---------|-------|
| ADC Lowpass Filter | Passband                    | 0       | -       | 19.2    | kHz   |
|                    | Stopband                    | 28.8    |         |         | kHz   |
|                    | Stopband Rejection          |         | -76.0   |         | dB    |
|                    | Passband Frequency Response |         | ±0.20   |         | dB    |
| DAC Lowpass Filter | Passband                    | 0       | -       | 19.2    | kHz   |
|                    | Stopband                    | 28.8    |         |         | kHz   |
|                    | Stopband Rejection          |         | -78.5   |         | dB    |
|                    | Passband Frequency Response |         | ±0.20   |         | dB    |

### 9.1.4. S/PDIF Input/Output Characteristics

DVDD= 3.3V, T<sub>ambient</sub>=25°C, with 75Ω external load.

**Table 74. S/PDIF Input/Output Characteristics**

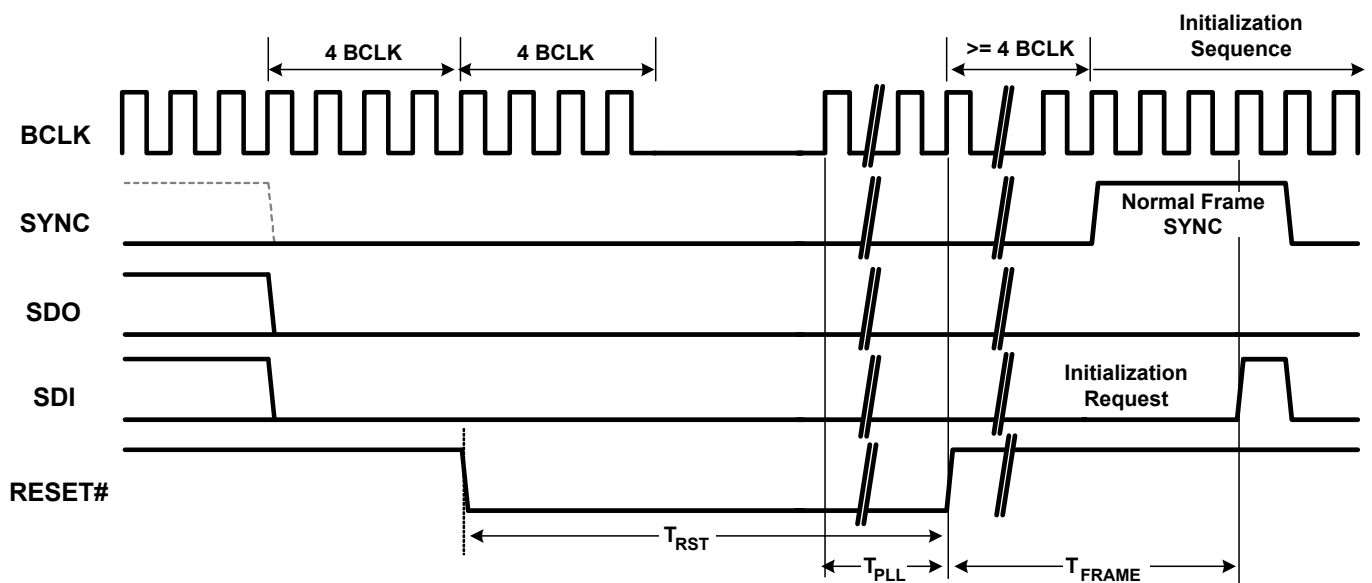
| Parameter                    | Symbol          | Minimum | Typical | Maximum | Units |
|------------------------------|-----------------|---------|---------|---------|-------|
| S/PDIF-OUT High Level Output | V <sub>OH</sub> | 3.0     | 3.3     | -       | V     |
| S/PDIF-OUT Low Level Output  | V <sub>OL</sub> | -       | 0       | 0.3     | V     |
| S/PDIF-IN High Level Input   | V <sub>IH</sub> | 1.85    | -       | -       | V     |
| S/PDIF-IN Low Level Input    | V <sub>IL</sub> | -       | -       | 1.45    | V     |
| S/PDIF-IN Bias Level         | V <sub>t</sub>  | -       | 1.65    | -       | V     |

## 9.2. AC Characteristic

### 9.2.1. Link Reset and Initialization Timing

**Table 75. Link Reset and Initialization Timing**

| Parameter                                                   | Symbol      | Minimum | Typical | Maximum | Units      |
|-------------------------------------------------------------|-------------|---------|---------|---------|------------|
| RESET# Active Low Pulse Width                               | $T_{RST}$   | 1.0     | -       | -       | $\mu s$    |
| RESET# Inactive to BCLK<br>Startup delay for PLL ready time | $T_{PLL}$   | 20      | -       | -       | $\mu s$    |
| SDI Initialization Request                                  | $T_{FRAME}$ | -       | -       | 1       | Frame Time |

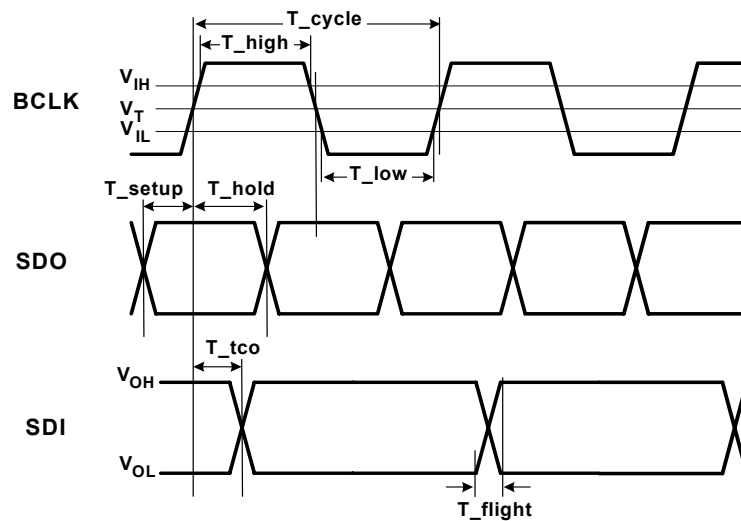


**Figure 15. Link Reset and Initialization Timing**

## 9.2.2. Link Timing Parameters at the Codec

**Table 76. Link Timing Parameters at the Codec**

| Parameter                                                        | Symbol              | Minimum        | Typical | Maximum        | Units     |
|------------------------------------------------------------------|---------------------|----------------|---------|----------------|-----------|
| BCLK Frequency                                                   |                     | -              | 24.0    | -              | MHz       |
| BCLK Period                                                      | $T_{\text{cycle}}$  | -              | 41.67   | -              | ns        |
| BCLK Jitter                                                      | $T_{\text{jitter}}$ | -              | -       | 2.0            | ns        |
| BCLK High Pulse Width                                            | $T_{\text{high}}$   | 18.75<br>(45%) | -       | 22.91<br>(55%) | ns<br>(%) |
| BCLK Low Pulse Width                                             | $T_{\text{low}}$    | 18.75<br>(45%) | -       | 22.91<br>(55%) | ns<br>(%) |
| SDO Setup Time at Both Rising and Falling Edge of BCLK           | $T_{\text{setup}}$  | 2.1            | -       | -              | ns        |
| SDO Hold Time at Both Rising and Falling Edge of BCLK            | $T_{\text{hold}}$   | 2.1            | -       | -              | ns        |
| SDI Valid Time After Rising Edge of BCLK (1: 50pF external load) | $T_{\text{tco}}$    | -              | 7.5     | 8.0            | ns        |
| SDI Flight Time                                                  | $T_{\text{flight}}$ | -              | 2.0     | -              | ns        |


**Figure 16. Link Signals Timing**

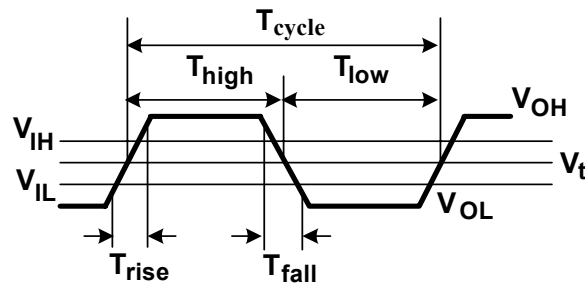
### 9.2.3. S/PDIF Output and Input Timing

**Table 77. S/PDIF Output and Input Timing**

| Parameter                                 | Symbol              | Minimum     | Typical     | Maximum     | Units  |
|-------------------------------------------|---------------------|-------------|-------------|-------------|--------|
| S/PDIF-OUT Frequency <sup>*1</sup>        | -                   | -           | 3.072       | -           | MHz    |
| S/PDIF-OUT Period <sup>*1</sup>           | $T_{\text{cycle}}$  | -           | 325.6       | -           | ns     |
| S/PDIF-OUT Jitter                         | $T_{\text{jitter}}$ | -           | -           | 4           | ns     |
| S/PDIF-OUT High Level Width <sup>*1</sup> | $T_{\text{High}}$   | 156.2 (48%) | 162.8 (50%) | 169.2 (52%) | ns (%) |
| S/PDIF-OUT Low Level Width <sup>*1</sup>  | $T_{\text{Low}}$    | 156.2 (48%) | 162.8 (50%) | 169.2 (52%) | ns (%) |
| S/PDIF-OUT Rising Time                    | $T_{\text{rise}}$   | -           | 2.0         | -           | ns     |
| S/PDIF-OUT Falling Time                   | $T_{\text{fall}}$   | -           | 2.0         | -           | ns     |
| S/PDIF-IN Period <sup>*2</sup>            | $T_{\text{cycle}}$  | -           | 325.6       | -           | ns     |
| S/PDIF-IN Jitter                          | $T_{\text{jitter}}$ | -           | -           | 10          | ns     |
| S/PDIF-IN High Level Width <sup>*2</sup>  | $T_{\text{High}}$   | 146.4 (45%) | 162.8 (50%) | 179 (55%)   | ns (%) |
| S/PDIF-IN Low Level Width <sup>*2</sup>   | $T_{\text{Low}}$    | 146.4 (45%) | 162.8 (50%) | 179 (55%)   | ns (%) |

<sup>\*1</sup>: Bit parameters for 48kHz sample rate of S/PDIF-OUT

<sup>\*2</sup>: Bit parameters for 48kHz sample rate of S/PDIF-IN


**Figure 17. Output and Input Timing**

### 9.2.4. Test Mode

The ALC883 series does not support codec test mode or Automatic Test Equipment (ATE) mode.

### 9.3. Analog Performance

Standard Test Conditions

- $T_{\text{ambient}}=25^{\circ}\text{C}$ ,  $DVDD=3.3\text{V} \pm 5\%$ ,  $AVDD=5.0\text{V} \pm 5\%$
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10K $\Omega$ /50pF load; Test bench Characterization BW:10Hz~22kHz, 0dB attenuation

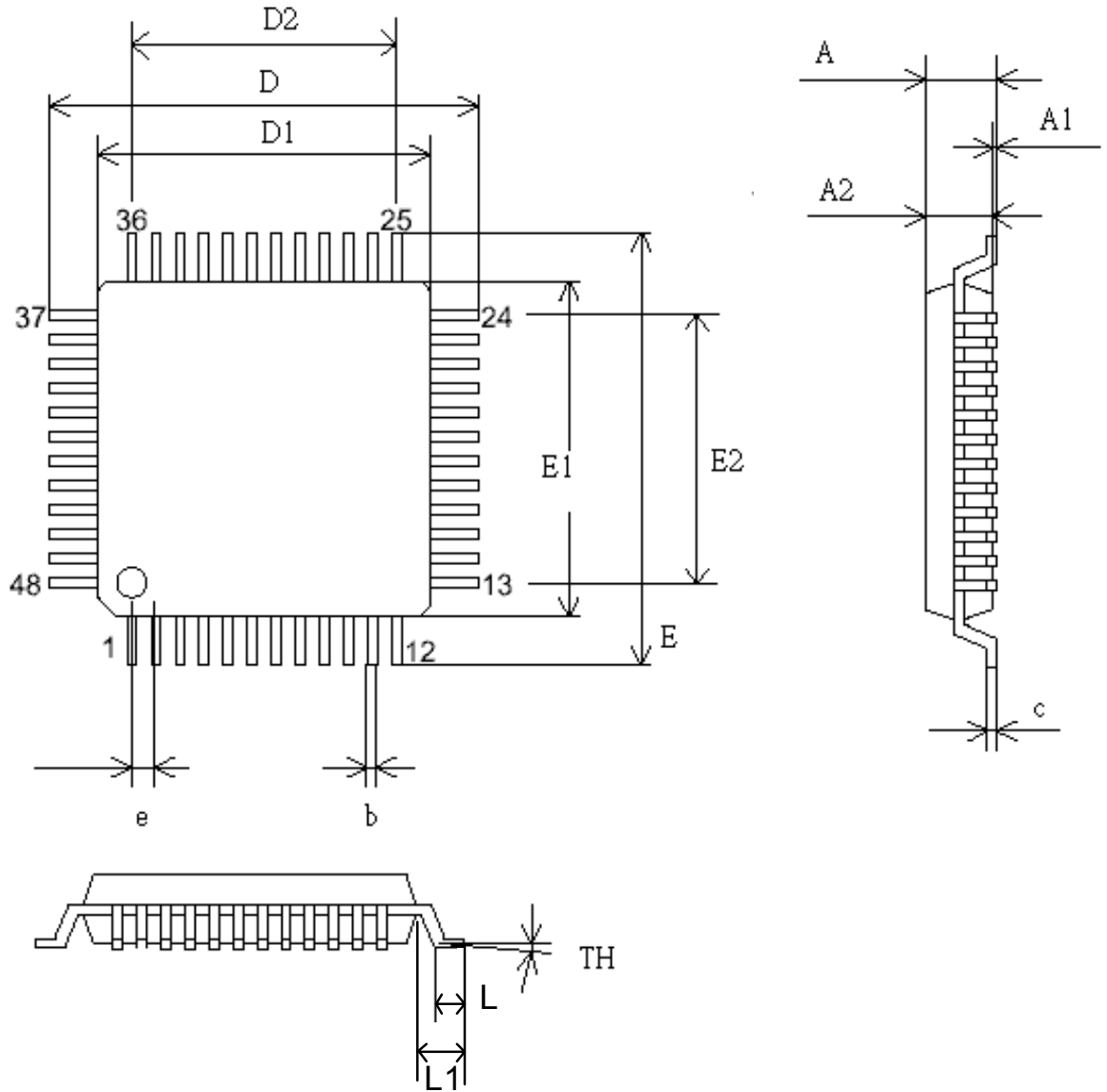
**Table 78. Analog Performance**

| Parameter                                       | Min  | Typical | Max    | Units      |
|-------------------------------------------------|------|---------|--------|------------|
| Full Scale Input Voltage                        |      |         |        |            |
| All Inputs (gain=0dB)                           | -    | 1.6     | -      | Vrms       |
| All ADC                                         | -    | 1.1     | -      | Vrms       |
| Full Scale Output Voltage                       |      |         |        |            |
| All DAC                                         | -    | 1.3     | -      | Vrms       |
| S/N (A Weighted)                                |      |         |        |            |
| Analog Inputs to Outputs                        | -    | 95      | -      | dB FSA     |
| All ADC                                         | -    | 85      | -      | dB FSA     |
| All DAC                                         | -    | 95      | -      | dB FSA     |
| THD+N                                           |      |         |        |            |
| Analog Inputs to Outputs                        | -    | -88     | -      | dB FS      |
| ADC                                             | -    | -78     | -      | dB FS      |
| All DAC                                         | -    | -86     | -      | dB FS      |
| Frequency Response                              |      |         |        |            |
| Mixers                                          | 10   | -       | 22,000 | Hz         |
| ADC, DAC                                        | 16   | -       | 19,200 | Hz         |
| Power Supply Rejection                          | -    | -40     | -      | dB         |
| Total Out-of-Band Noise (28.8kHz~100kHz)        | -    | -60     | -      | dB         |
| Amplifier Gain Step                             | -    | 1.5     | -      | dB         |
| Crosstalk Between Input Channels                | -    | -80     |        | dB         |
| Input Impedance (gain=0dB)                      |      | 47      |        | K $\Omega$ |
| Output Impedance                                |      |         |        |            |
| Amplified Output                                |      | 5       |        | $\Omega$   |
| Non-amplified Output                            |      | 150     |        | $\Omega$   |
| Digital Power Supply Current (normal operation) |      |         |        |            |
| DVDD=3.3V                                       | -    | 35      | -      | mA         |
| Digital Power Supply Current (power down mode)  |      |         |        |            |
| DVDD=3.3V                                       | -    | 0.92    | -      | mA         |
| Analog Power Supply Current (normal operation)  |      |         |        |            |
| AVDD=5.0V                                       | -    | 55      | -      | mA         |
| Analog Power Supply Current (power down mode)   |      |         |        |            |
| AVDD=5.0V                                       | -    | 1.76    | -      | mA         |
| VREFOUTx Output Voltage                         | 2.25 | 2.50    | 3.75   | V          |
| VREFOUTx Output Current                         |      | 5       |        | mA         |

## 10. Application Circuits

Designers are suggested to contact Realtek to get the latest application circuits. To get the best compatibility in hardware design and software driver, any modifications of application circuits should be confirmed by Realtek. Realtek may update the latest application circuits onto our web site ([www.realtek.com.tw](http://www.realtek.com.tw)) without modifying this datasheet.

## 11. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

## 11.1. Mechanical Dimensions Notes

| SYMBOL | MILLIMETER |      |      | INCH       |        |       |
|--------|------------|------|------|------------|--------|-------|
|        | MIN        | TYP  | MAX  | MIN.       | TYP    | MAX   |
| A      |            |      | 1.60 |            |        | 0.063 |
| A1     | 0.05       |      | 0.15 | 0.002      |        | 0.006 |
| A2     | 1.35       | 1.40 | 1.45 | 0.053      | 0.055  | 0.057 |
| c      | 0.09       |      | 0.20 | 0.004      |        | 0.008 |
| D      | 9.00 BSC   |      |      | 0.354 BSC  |        |       |
| D1     | 7.00 BSC   |      |      | 0.276 BSC  |        |       |
| D2     | 5.50       |      |      | 0.217      |        |       |
| E      | 9.00 BSC   |      |      | 0.354 BSC  |        |       |
| E1     | 7.00BSC    |      |      | 0.276 BSC  |        |       |
| E2     | 5.50       |      |      | 0.217      |        |       |
| b      | 0.17       | 0.20 | 0.27 | 0.007      | 0.008  | 0.011 |
| e      | 0.50 BSC   |      |      | 0.0196 BSC |        |       |
| TH     | 0°         | 3.5° | 7°   | 0°         | 3.5°   | 7°    |
| L      | 0.45       | 0.60 | 0.75 | 0.018      | 0.0236 | 0.030 |
| L1     |            | 1.00 |      |            | 0.0393 |       |

|                                |          |           |
|--------------------------------|----------|-----------|
| TITLE: LQFP-48 (7.0x7.0x1.6mm) |          |           |
| PACKAGE OUTLINE DRAWING,       |          |           |
| FOOTPRINT 2.0mm                |          |           |
| LEADFRAME MATERIAL             |          |           |
| APPROVE                        | DOC. NO. |           |
|                                | VERSION  | 02        |
| CHECK                          | DWG NO.  | PKG-C-065 |
|                                | DATE     |           |
| REALTEK SEMICONDUCTOR CORP.    |          |           |

## 12. Ordering Information

**Table 79. Ordering Information**

| Part Number | Description                                                        | Status |
|-------------|--------------------------------------------------------------------|--------|
| ALC883-GR   | LQFP-48 with 'Green' package                                       | Sample |
| ALC883DD-GR | ALC883-GR + Dolby® Digital Live + DTS CONNECT™ (software features) | N/A    |

*Note 1: See page 6 for Green package and version identification.*

*Note 2: Above parts are tested under AVDD = 5.0V. If customers have a lower AVDD request, please contact Realtek sales representatives or agents.*

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