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RTD1073DD-GR
RTD1073DA-GR

HD H.264/VC1/MPEG/RM DECODER WITH ETHERNET AND HDMI

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTD1073 controller ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/02/27	First release.
1.1	2009/03/20	Updated product numbers (see section 19 Ordering Information, page 45).

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1. General Description

The RTD1073DD-GR/RTD1073DA-GR is a highly integrated SoC for Consumer Electronic products requiring High Definition Media Playback, Wireless/Wired Networking, and Mass Storage capabilities.

Main features of the RTD1073 include HD MPEG1/2/4 & HD JPEG Decoder, HD AVC/VC-1 Decoder, RM/RMVB Decoder, AV Streaming/Transmission via Ethernet & WiFi, TV Encoder with CVBS/ YPbPr/SCART out, I^2S, SPDIF out, HDMI Transmitter and PHY, OTP (One-Time Programmable ROM), dual USB2.0 Host or one USB2.0 Host/Device with dual port integrated PHY, NAND/NOR flash controller, Dual SATA, and Fast Ethernet MAC and PHY.

2. Features

2.1. Hardware Features

- System and Peripherals
  - 400MHz MIPS24Kc processor
  - Video DSP with HW acceleration
  - Audio DSP with HW acceleration
  - Supports up to 128MB DDR2 SDRAM with 16-bit data interface
  - Supports Serial Flash with 1-bit data interface
  - NAND/NOR Flash controller
  - Boot-ROM and OTP (One-Time Programmable ROM) for Secure-Boot and Key storage
  - Integrates dual channel SATA 2.0 with PHY
  - Fast Ethernet MAC and PHY
  - Integrates dual USB2.0 High Speed Host controller, or one Host/Device controller, and Dual PHY
  - Supports UART/IR/I^{2}C/GPIO/ EJTAG/VFD/RTC
- Audio Interface and Function
  - I^{2}S interfaces for Audio output
  - IEC-958 (SPDIF) digital audio output
  - 7.1 down-mix
  - MPEG I Layer 1, 2, 3 (2-CH) and MPEG II Layer 1, 2 (Multi-Channel)
  - LPCM, ADPCM, FLAC, AAC, WAV, and OGG Vorbis
  - DTS HD Master Audio, LBR
  - Dolby® Digital Plus, TrueHD
  - RA1/RA-cook/RA-lossless
  - WMA/WMA Pro, Dolby® Digital AC3 and DTS® (Licensee Only)
- Video Interface
  - TV encoder with four 12-bit video D/A converters
  - NTSC and PAL TV systems
  - Composite analog video outputs
  - Component (YPbPr or RGB) analog video output
  - Simultaneous Composite and YPbPr output
  - Simultaneous SD/HD output
  - VGA/XVGA/SVGA output
  - HDMI V1.3 transmitter with CEC
  - Supports SCART output
  - 3D De-interlacer
  - Bitmap OSD
- Video and Picture Function
  - MPEG1, VCD 1.0/2.0, SVCD
  - Supports HD MPEG2 (up to MP@HL 1080i), ISO/IFO/VOB/TS
  - Supports HD MPEG4 SP/ASP (720p/1080i/1080p), Xvid
  - H.264 BP@L3, MP@L4.1, HP@L4.1
  - WMV9/VC-1 AP@L3
  - RealNetworks (RM/RMVB) 8/9/10, up to 720@30P
  - DivX3/4/5/6 (Licensee Only)
  - HD JPEG with unlimited resolution (40M-pixel tested)

- Full-pixel JPEG decode with high resolution zoom-in
- De-blocking/De-ringing Filter
- Video upscaling from SD to HD (720p/1080i/1080p)
- Supports PIP/POP

- Copy Protection
  - CSS
  - CGMS-A
  - HDCP
  - Microsoft DRM

2.2. Software Features

- Operating System: Linux
- HDD File System: FAT16/FAT32/NTFS/EXT3
- Media Browser and Player (Movie, Music, and Photo)
- Supports Subtitle: SRT, SMI, SUB, SSA, IDX+SUB
- Photo slideshow with background music
- Photo slideshow with transition effects: Cross fade, Left to right, top to bottom, waterfall, snake, dissolve, Strip left down, all effects shuffle
- Network applications

3. System Applications

- HD Media Player
- Digital Media Adaptor/Server
- Networked Media Module for Embedded CE devices

3.1. Application Diagram

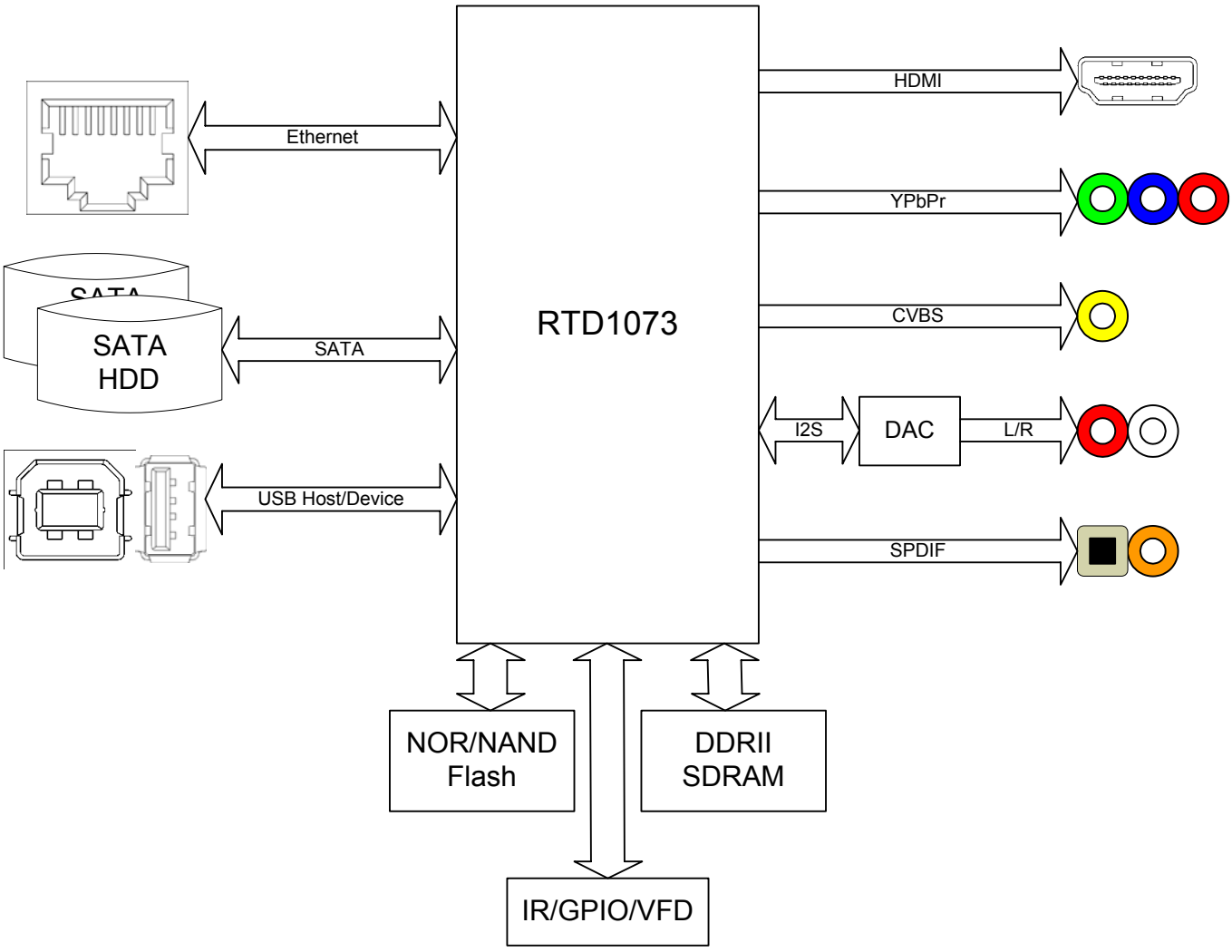

Figure 1. Application Diagram

4. Block Diagram

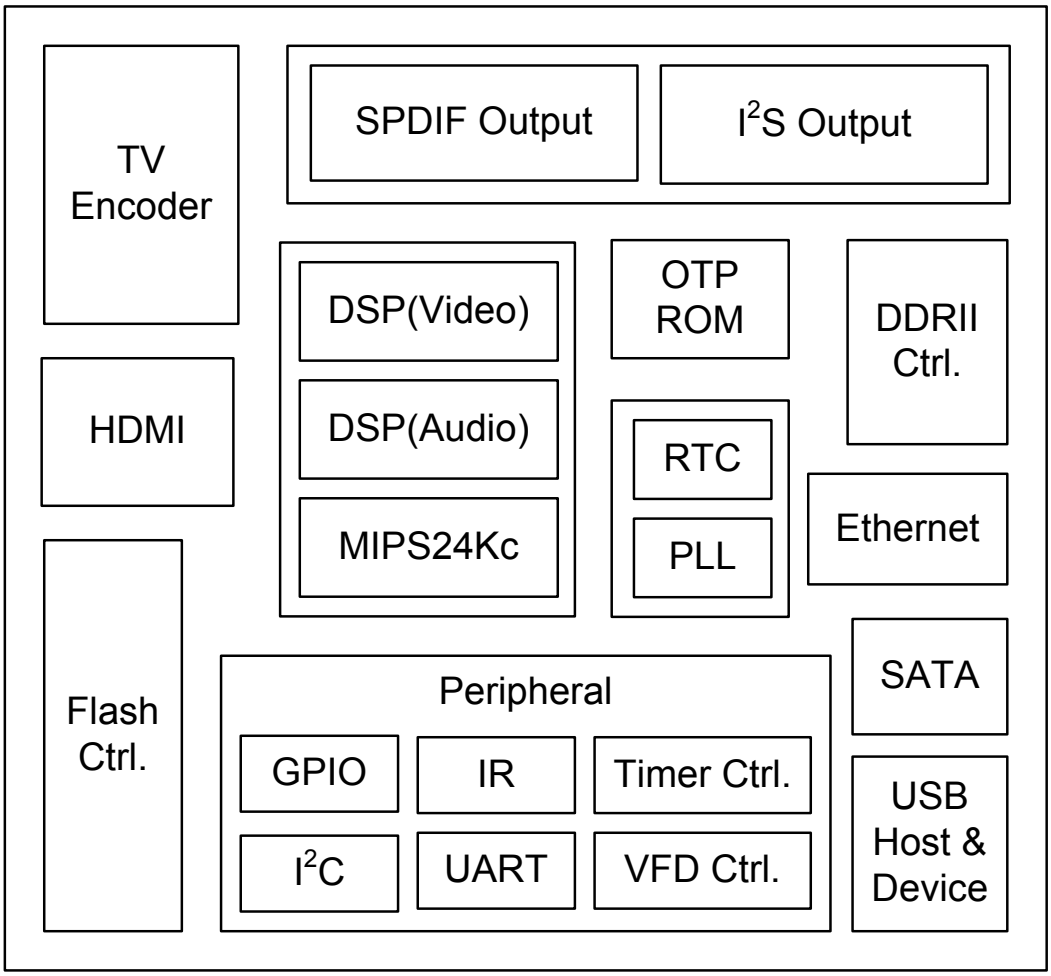

Figure 2. Block Diagram

5. Pin Assignments

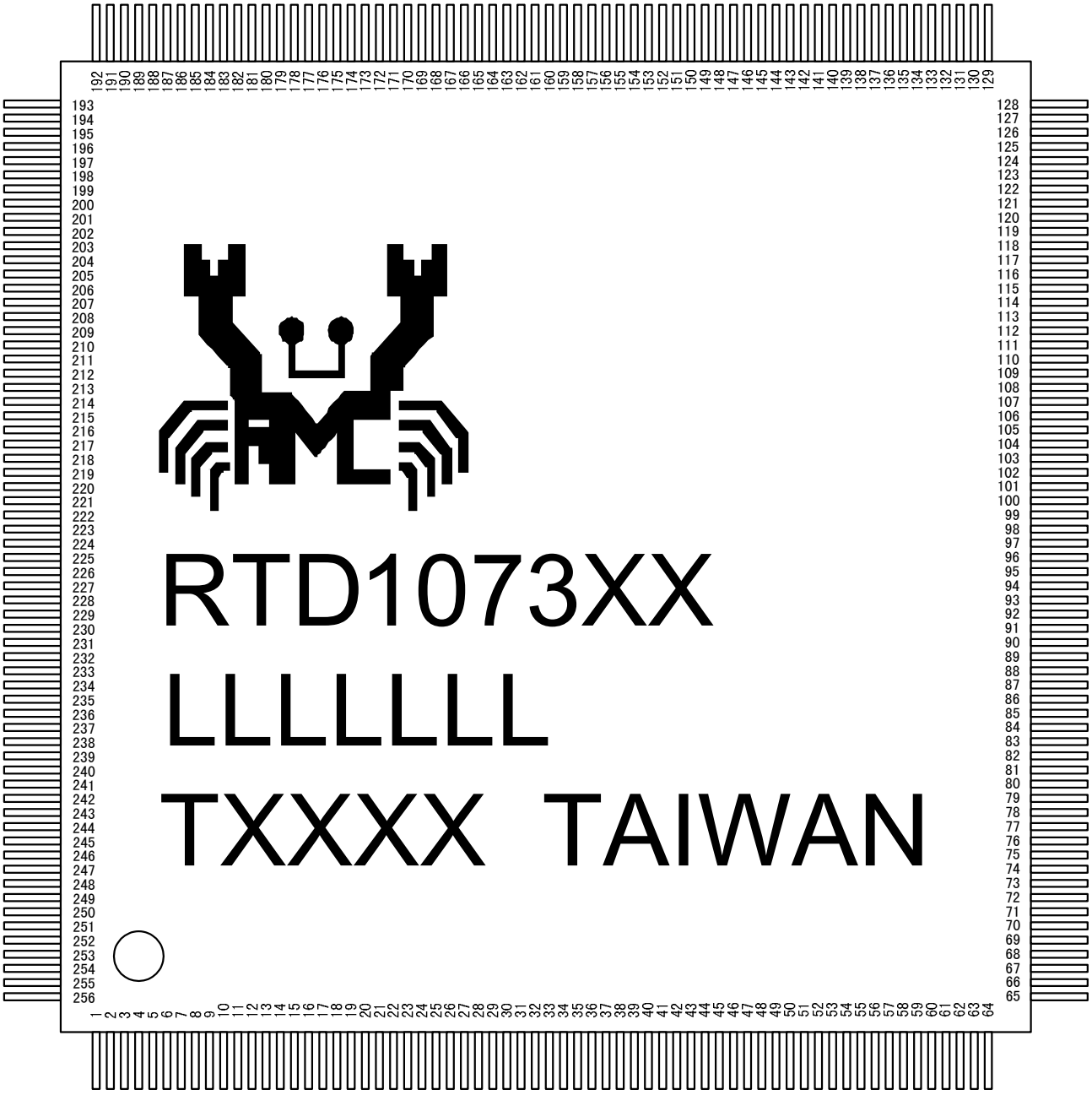

Figure 3. Package Assignments

5.1. Package and Version Identification

XX in the model number indicates DD or DA model. Green package is indicated by a ‘G’ in the location marked ‘T’.

6. Pin Descriptions

DI: Digital Input

DO: Digital Output

DB: Digital Bidirectional

USB: Defined in USB Specification

TMDS: Defined in HDMI Specification

GND: Ground

AI: Analog Input

AO: Analog Output

AB: Analog Bidirectional

SATA: Defined in SATA Specification

SSTL18: Defined in DDRII Specification

PWR: Power Supply

Table 1. Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	CEC	AB	HDMI Consumer Electronic Channel
2	GND	PWR	Ground for HDMI
3	TXC-	AO	HDMI Output Clock Pair
4	TXC+	AO	HDMI Output Clock Pair
5	3.3V	PWR	Power for HDMI
6	TX0-	AO	HDMI Output Data Pair 0
7	TX0+	AO	HDMI Output Data Pair 0
8	GND	PWR	Ground for HDMI
9	TX1-	AO	HDMI Output Data Pair 1
10	TX1+	AO	HDMI Output Data Pair 1
11	3.3V	PWR	Power for HDMI
12	TX2-	AO	HDMI Output Data Pair 2
13	TX2+	AO	HDMI Output Data Pair 2
14	GND	PWR	Ground for HDMI
15	1.2V	PWR	Power for Ethernet
16	TXP	AO	Transmit Positive Output
17	TXN	AO	Transmit Negative Output
18	GND	PWR	Ground for Ethernet
19	RXP	AI	Receiver Positive Input
20	RXN	AI	Receiver Negative Input
21	GND	PWR	Ground for Ethernet
22	3.3V	PWR	Power for Ethernet
23	1.2V	PWR	Core Power
24	LED_RXTX	DO	Indicator of TX/RX Packet
25	LED_LINK	DO	Indicator of Link
26	HPD	DI	HDMI Hot Plug In
27	GPIO42	DB	General Purpose I/O
28	GPIO43	DB	General Purpose I/O

Pin No.	Pin Name	I/O	Description
29	GPIO44	DB	General Purpose I/O
30	1.2V	PWR	Core Power
31	1.2V	PWR	Core Power
32	S_FLASH	DI	Select Serial Flash
33	3.3V	PWR	I/O Pad Power
34	I2C_SDA0	DB	I^2C Serial Data Signal
35	I2C_SCL0	DB	I^2C Serial Clock Signal
36	1.2V	PWR	Core Power
37	VDDP	PWR	Power for OTP, 3.3V
38	NC	-	Not Connected
39	1.2V	PWR	Power for USB
40	USB0_DM	AB	USB 0 D- Signal
41	USB0_DP	AB	USB 0 D+ Signal
42	3.3V	PWR	Power for USB
43	GND	PWR	Ground for USB
44	GND	PWR	Ground for USB
45	USB1_DM	AB	USB 1 D- Signal
46	USB1_DP	AB	USB 1 D+ Signal
47	1.2V	PWR	Power for USB
48	1.2V	PWR	Core Power
49	1.2V	PWR	Power for SATA
50	SATA0_HSIP	AI	First SATA RX+ Signal
51	SATA0_HSIN	AI	First SATA RX- Signal
52	GND	PWR	Ground for SATA
53	1.2V	PWR	Power for SATA
54	SATA0_HSON	AO	First SATA TX- Signal
55	SATA0_HSOP	AO	First SATA TX+ Signal
56	GND	PWR	Ground for SATA
57	1.2V	PWR	Power for SATA
58	SATA1_HSIP	AI	Second SATA RX+ Signal
59	SATA1_HSIN	AI	Second SATA RX- Signal
60	GND	PWR	Ground for SATA
61	1.2V	PWR	Power for SATA
62	SATA1_HSON	AO	Second SATA TX- Signal
63	SATA1_HSOP	AO	Second SATA TX+ Signal
64	GND	PWR	Ground for SATA
65	1.2V	PWR	Core Power
66	USB0_OverCur_FLAG	DI	USB 0 Over-Current Detect
67	USB1_OverCur_FLAG	DI	USB 1 Over-Current Detect (Host Mode)
	USB1_VBUS	DI	USB 1 VBUS-In Detect (Device Mode)
68	RESET_N	DI	Chip Reset, Schmitt Trigger Input, Internally Weakly Pull-Up
69	UART_TX0	DO	UART 0 Transmit Data Output
	I2C_SDA1	DB	I^2C Serial Data Signal

Pin No.	Pin Name	I/O	Description
70	UART_RX0	DI	UART 0 Receive Data Input
	I2C_SCL1	DB	I^2C Serial Clock Signal
71	N_FLASH	DI	Select NAND/NOR Flash, 1=NAND
72	VFD_D	DB	Serial Data Input/Output, Open-Drain, 5V Tolerant
73	VFD_CLK	DO	VFD Clock, Open-Drain
74	VFD_CS_N	DO	Data Enable, Open-Drain
75	IR_IN	DI	Infrared Input from IR Receiver, 5V Tolerant
76	1.2V	PWR	Core Power
77	1.2V	PWR	Core Power
78	3.3V	PWR	I/O Pad Power
79	NF_RDY	DI	NAND Flash Ready
80	NF_CE_N0	DO	NAND Flash Chip Enable
81	SPI_CE_N	DO	Serial NOR Flash Chip Select Output
82	NF_CE_N1	DO	NAND Flash Chip Enable
83	1.2V	PWR	Core Power
84	1.2V	PWR	Core Power
85	DVRI	PWR	I/O Reference Voltage of SSTL18 Interface
86	DQ4	DB	DDRII Data Bus
87	DQ1	DB	DDRII Data Bus
88	1.8V	PWR	DDRII Pad Power
89	DQ6	DB	DDRII Data Bus
90	DQ12	DB	DDRII Data Bus
91	DQ9	DB	DDRII Data Bus
92	DQ14	DB	DDRII Data Bus
93	1.8V	PWR	DDRII Pad Power
94	DUDM	DO	DDRII DQ[15:8] Data Mask
95	DQ11	DB	DDRII Data Bus
96	DLDM	DO	DDRII DQ[7:0] Data Mask
97	DQ3	DB	DDRII Data Bus
98	1.8V	PWR	DDRII Pad Power
99	DQ2	DB	DDRII Data Bus
100	DQ0	DB	DDRII Data Bus
101	DLDQS	DB	DDRII DQ[7:0] Data Strobe (Differential Pair)
102	DLDQS_N	DB	DDRII Inverse DQ[7:0] Data Strobe (Differential Pair)
103	1.8V	PWR	DDRII Pad Power
104	DQ10	DB	DDRII Data Bus
105	DQ8	DB	DDRII Data Bus
106	DUDQS	DB	DDRII DQ[15:8] Data Strobe (Differential Pair)
107	DUDQS_N	DB	DDRII Inverse DQ[15:8] Data Strobe (Differential Pair)
108	1.8V	PWR	DDRII Pad Power
109	DQ15	DB	DDRII Data Bus
110	DQ13	DB	DDRII Data Bus
111	DQ7	DB	DDRII Data Bus
112	DQ5	DB	DDRII Data Bus

Pin No.	Pin Name	I/O	Description
113	1.8V	PWR	DDRII Pad Power
114	1.2V	PWR	Core Power
115	NC	-	Not Connected
116	DCK	DO	DDRII Clock (Differential Clock)
117	DCK_N	DO	DDRII Inverse Clock (Differential Clock)
118	DODT	DO	DDRII On Die Termination
119	1.8V	PWR	DDRII Pad Power
120	DRAS_N	DO	DDRII Row Address Select
121	DCS_N	DO	DDRII Chip Select
122	DCAS_N	DO	DDRII Column Address Select
123	DA0	DO	DDRII Address Bus
124	DA2	DO	DDRII Address Bus
125	DA4	DO	DDRII Address Bus
126	DA6	DO	DDRII Address Bus
127	DA8	DO	DDRII Address Bus
128	DA11	DO	DDRII Address Bus
129	DCKE	DO	DDRII Clock Enable
130	1.8V	PWR	DDRII Pad Power
131	DWE_N	DO	DDRII Write Enable
132	DBANK2	DO	DDRII Bank Address
133	DBANK1	DO	DDRII Bank Address
134	DBANK0	DO	DDRII Bank Address
135	DA1	DO	DDRII Address Bus
136	DA10	DO	DDRII Address Bus
137	DA5	DO	DDRII Address Bus
138	DA3	DO	DDRII Address Bus
139	DA9	DO	DDRII Address Bus
140	DA7	DO	DDRII Address Bus
141	1.8V	PWR	DDRII Pad Power
142	DA12	DO	DDRII Address Bus
143	1.2V	PWR	Core Power
144	1.2V	PWR	Core Power
145	GND	PWR	Ground for PLL
146	3.3V	PWR	Power for PLL
147	3.3V	PWR	Power for PLL
148	XOUT	AO	System Clock 27MHz
149	XIN	AI	System Clock 27MHz
150	GND	PWR	Ground for PLL
151	RTC_XIN	AI	Real-Time Clock 32.768kHz
152	RTC_XOUT	AO	Real-Time Clock 32.768kHz
153	RTC_VDD	PWR	Power for RTC, 3.3V
154	1.2V	PWR	Core Power
155	SPI_SCK	DO	Serial NOR Flash Clock
156	SPI_SO	DI	Serial NOR Flash Data Output

Pin No.	Pin Name	I/O	Description
157	SPI_SEL	DI	Select Read Command for Boot-Up
158	SPI_WP_N	DO	Serial NOR Flash Write Protect
159	SPI_SI	DO	Serial NOR Flash Data Input
160	NC	-	Not Connected
161	NC	-	Not Connected
162	NC	-	Not Connected
163	NC	-	Not Connected
164	NC	-	Not Connected
165	3.3V	PWR	I/O Pad Power
166	NF_RD_N	DO	NAND Flash Read Enable
167	NF_CLE	DO	NAND Flash Command Latch Enable
168	NF_ALE	DO	NAND Flash Address Latch Enable
169	NF_WR_N	DO	NAND Flash Write Enable
170	NF_DD0	DB	NAND Flash Data Bus
171	NF_DD1	DB	NAND Flash Data Bus
172	NF_DD2	DB	NAND Flash Data Bus
173	NF_DD3	DB	NAND Flash Data Bus
174	1.2V	PWR	Core Power
175	NC	-	Not Connected
176	3.3V	PWR	I/O Pad Power
177	NF_DD4	DB	NAND Flash Data Bus
178	NF_DD5	DB	NAND Flash Data Bus
179	NF_DD6	DB	NAND Flash Data Bus
180	NF_DD7	DB	NAND Flash Data Bus
181	NC	-	Not Connected
182	NC	-	Not Connected
183	NC	-	Not Connected
184	3.3V	PWR	I/O Pad Power
185	NC	-	Not Connected
186	NC	-	Not Connected
187	NC	-	Not Connected
188	NC	-	Not Connected
189	NC	-	Not Connected
190	NC	-	Not Connected
191	NC	-	Not Connected
192	VGA_HSYNC	DO	VGA Horizontal Synchronization Output
193	VGA_VSYNC	DO	VGA Vertical Synchronization Output
194	3.3V	PWR	I/O Pad Power
195	NC	-	Not Connected
196	1.2V	PWR	Core Power
197	GPIO78	DB	General Purpose I/O
198	GPIO77	DB	General Purpose I/O
199	GPIO76	DB	General Purpose I/O
200	1.2V	PWR	Core Power

Pin No.	Pin Name	I/O	Description
201	GPIO75	DB	General Purpose I/O
202	GPIO74	DB	General Purpose I/O
203	GPIO73	DB	General Purpose I/O
204	3.3V	PWR	I/O Pad Power
205	GPIO72	DB	General Purpose I/O
206	GPIO71	DB	General Purpose I/O
207	GPIO67	DB	General Purpose I/O
208	GPIO69	DB	General Purpose I/O
209	GPIO68	DB	General Purpose I/O
210	GPIO83	DB	General Purpose I/O
211	GPIO79	DB	General Purpose I/O
212	GPIO81	DB	General Purpose I/O
213	1.2V	PWR	Core Power
214	NC	-	Not Connected
215	UART_RX1	DI	UART 1 Receive Data Input
216	UART_TX1	DO	UART 1 Transmit Data Output
217	TESTMODE	DI	Select Test Mode
218	GPIO93	DB	General Purpose I/O
219	GPIO94	DB	General Purpose I/O
220	NC	-	Not Connected
221	NC	-	Not Connected
222	NC	-	Not Connected
223	3.3V	PWR	I/O Pad Power
224	NC	-	Not Connected
225	GPIO46	DB	General Purpose I/O
226	GPIO47	DB	General Purpose I/O
227	GPIO48	DB	General Purpose I/O
228	GPIO49	DB	General Purpose I/O
229	GPIO50	DB	General Purpose I/O
230	GPIO51	DB	General Purpose I/O
231	GPIO52	DB	General Purpose I/O
232	1.2V	PWR	Core Power
233	GPIO53	DB	General Purpose I/O
234	GPIO45	DB	General Purpose I/O
235	EJTAG_TDO	DO	EJTAG Test Data Output
236	EJTAG_TDI	DI	EJTAG Test Data Input
237	EJTAG_TMS	DI	EJTAG Test Mode Select Input
238	3.3V	PWR	I/O Pad Power
239	EJTAG_TCK	DI	EJTAG Test Clock Input
240	AO_D0	DO	I^2S Serial Data Output for Left & Right Channels
	EJTAG_TRST_N	DI	EJTAG Test Reset Input
241	AO_LRCK	DO	I^2S Word Select Clock Output to DAC
242	AO_BCLK	DO	I^2S Bit Clock Output to DAC

Pin No.	Pin Name	I/O	Description
243	AO_MCLK	DO	Main Clock Output to DAC
244	AO_SPDIF	DO	IEC958 (SPDIF) Output
245	1.2V	PWR	Core Power
246	3.3V	PWR	Power for VDAC
247	VO_CVBS	AO	Analog Composite
248	NC	-	Not Connected
249	NC	-	Not Connected
250	GND	PWR	Ground for VDAC
251	REXT	AB	Bandgap Voltage of Whole Chip, Connect to GND via a 15KΩ, ±1% resistor
252	GND	PWR	Ground for VDAC
253	VO_CPr	AO	Component Analog Video Red or Pr
254	VO_CPb	AO	Component Analog Video Blue or Pb
255	VO_CY	AO	Component Analog Video Green or Luminance
256	3.3V	PWR	Power for VDAC
257	GND	PWR	E-PAD, Should be connected to Ground

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Windows Media DRM

Windows Media DRM 10 for Network Devices allows the RTD1073 to play back Windows Media–based protected content that resides on another computer on a network.

For details, contact Microsoft at: Microsoft Corporation, One Microsoft Way, Redmond, WA 98052-6399, USA. http://www.microsoft.com.

8. System Global Resources

8.1. Power Supply

It is important to provide adequate power and ground for high-speed digital and sensitive analog design. To achieve the best quality, power and ground pins are separated into several groups.

Table 2. Power Supply Specification

Pin Name	Min.	Typ.	Max.	Unit	Description
1.2V	-	1.2	-	V	Power Supply of Core Digital Logic
1.8V	-	1.8	-	V	Power Supply of SSTL18 I/O Pad
3.3V	-	3.3	-	V	Power Supply of I/O Pad or HW Block
RTC_VDD	1.0	3.3	-	V	Power Supply of RTC Block
DVRI	-	0.9	-	V	I/O Reference Voltage of SSTL18 Interface

8.2. Power Management

The RTD1073 provides a Sleep Mode that shuts down all PLLs and logic to save power during idle state. Sleep Mode is entered via a software instruction sequence, and exited by a hardware reset. External wake-up events may be selected to automatically generate a wake-up reset.

Some RTD1073 modules could be individually powered down by gating off their clock tree. Those modules can be powered on without resetting the whole chip.

8.3. Electrical Characteristics of LVTTL I/O Pads

Table 3. LVTTL Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	HIGH Level Input Voltage	2.0	-	-	V	-
V_{IL}	LOW Level Input Voltage	-	-	0.8	V	-
V_{OH}	HIGH Level Output Voltage	V_{CC}-0.2	V_{CC}	-	V	$-I_O = 20\mu A$
V_{OL}	LOW Level Output Voltage	-	-	0.4	V	$I_O = 4.0mA$
$\pm I_I$	Input Leakage Current	-	1	2	µA	$V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$

8.4. Reset, Clock, and PLL

Table 4. System Global Resources External Pin Description

Pin Name	IO Standard	Type	Description
RESET_N	LVTTL	DI	Chip Reset, Schmitt Trigger Input, Internal, Weakly Pulled-Up
XIN	Analog	AI	System Clock 27MHz
XOUT	Analog	AO	System Clock 27MHz
REXT	Analog	AB	Bandgap Voltage of Whole Chip, Connect to GND via a 15KΩ, ±1% Resistor

The external RESET_N signal is low-active, Schmitt trigger input. To take effect, it must be held low for at least 500ns. An external crystal (27MHz) is required for normal function, and the embedded PLL circuit will generate all necessary clock signals for various modules. The crystal accuracy should be under 30ppm to ensure the best quality.

SSC (Spread Spectrum Clock) technology is a useful feature for system designers to solve the EMI problem. For those modules that do not require fixed frequency, SSC has been used for a number of years with very good results.

8.5. Thermal Characteristics

Table 5. Thermal Characteristics

Parameter	Maximum	Unit
Thermal Resistance (θ_{JA}) @ 4 Layer PCB	TBD	°C/W
Thermal Resistance (θ_{JC}) @ 4 Layer PCB	TBD	°C/W

8.6. Power-On Sequence

Generally, the power-on sequence should be as follows:

- Apply 3.3V, 1.2V, and 1.8V
- Wait for power supplies to be stable
- Reset operation completes
- System boots up

The RTD1073 integrates a Power-On-Reset (POR) circuit to ensure the chip powers up in a default state. It monitors the status of 3.3V and 1.2V. The POR circuit reset will release after 2^{20} crystal clock cycles when both the V_{DD} and V_{CORE} are stable.

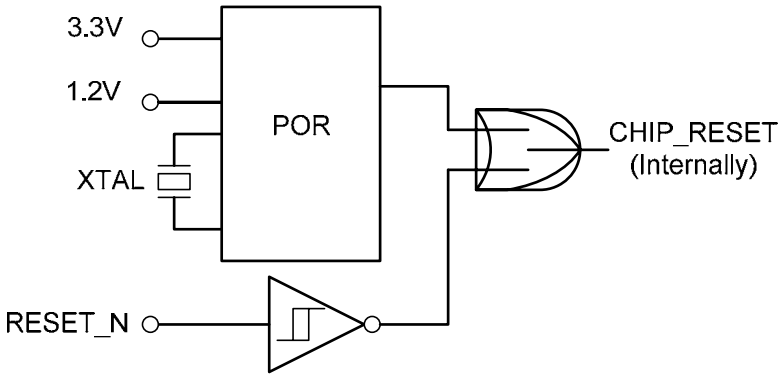


Figure 4. POR Circuit Diagram

The Power-On-Reset (POR) will assert a reset signal when the 3.3V or 1.2V fall below certain voltage levels. Refer to Figure 5, the sequence of applying 3.3V and 1.2V is suggested to be 3.3V leads 1.2V; that is, $t_1 > 0$.

1.8V is required to be stable before the end of the reset duration, that is, $t_2 > 0$.

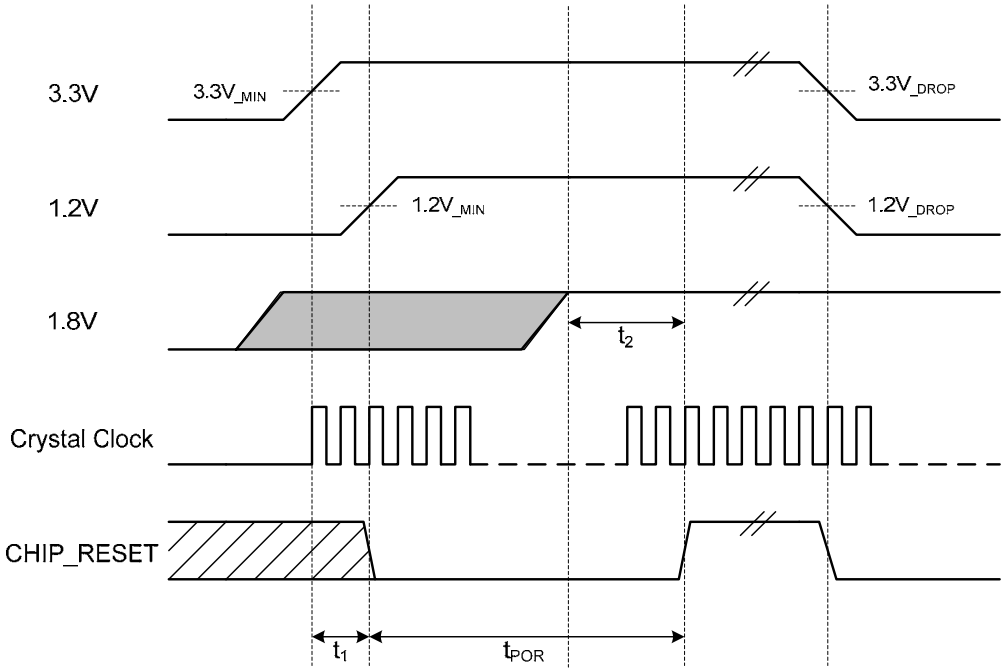


Figure 5. Power-On Sequence Timing Diagram

Table 6. POR Circuit Specification

Parameter	Description	TYP.	Unit
$3.3V_{\_MIN}$	Minimum Voltage to De-Assert POR	2.5	V
$1.2V_{\_MIN}$	Minimum Voltage to De-Assert POR	0.8	V
$3.3V_{\_DROP}$	Trigger Voltage to Assert POR	2.0	V
$1.2V_{\_DROP}$	Trigger Voltage to Assert POR	0.75	V
t_{POR}	POR Reset Time	2^{20}	Cycles

8.7. System Boot Up Considerations

Once the reset signal is released, the RTD1073 will fetch instructions from the external Flash ROM within 14 cycles. Before the first fetch operation, Flash ROM is required to be ready for reading. For modern serial/parallel Flash ROM, it needs some time (t_{RH}) to make itself ready for operation after power-on/reset. In a typical system, there are two possible scenarios:

- Power-On Reset: The whole system is powered-on from a power-off state. Generally, the t_{POR} is about 38ms, the value is far greater than t_{RH}, which is several micro seconds. In this condition, Flash ROM is already operational before the first instruction fetch, so there is no issue.
- Hard Reset: The system is in power-on state and receives a reset signal from the RESET_N pin. If Flash ROM could not be ready in 14 cycles, the system may malfunction due to an unknown instruction being fetched. The system designer should carefully handle this issue to prevent future mysterious bugs. The rule of thumb is to keep t_3 (refer to Figure 6) greater than t_{RH}. One simple approach is never to reset Flash ROM except via its own power-on-reset.

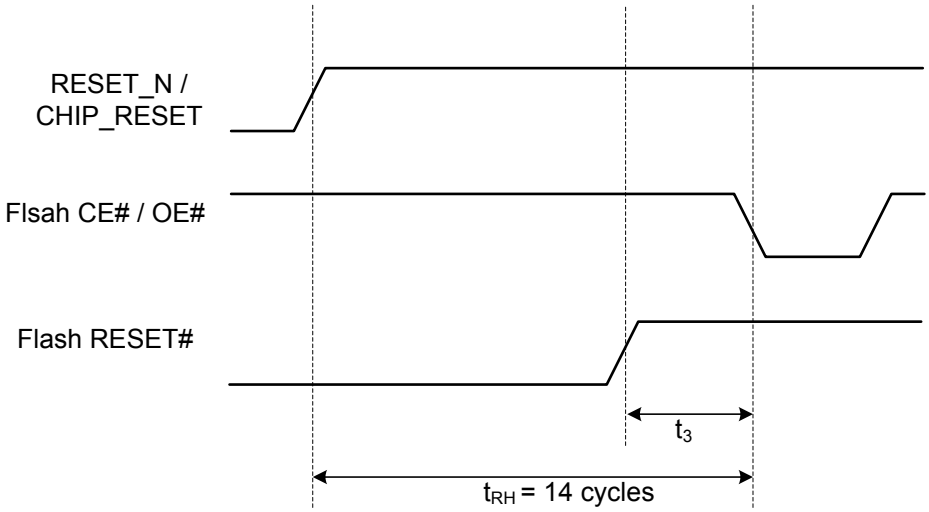


Figure 6. System Reset and Flash Reset

9. DDR2 Controller Unit

The RTD1073 DDR2 Controller Unit (DCU) provides memory control signals required for external DDR2 SDRAM access. With a 16-bit-wide DDR2 SDRAM, the DCU can access up to 128MB.

9.1. Features

- Supports up to 128MB
- 1.8V SSTL18 compatible I/O

9.2. DCU Block External Pin Description

Table 7. DCU Block External Pin Description

Pin Name	IO Standard	Type	Description
DCK	SSTL18	DO	Clock (Differential Clock)
DCK_N	SSTL18	DO	Inverse Clock (Differential Clock)
DCKE	SSTL18	DO	Clock Enable
DODT	SSTL18	DO	On Die Termination
DCS_N	SSTL18	DO	Chip Select
DRAS_N	SSTL18	DO	Row Address Select
DCAS_N	SSTL18	DO	Column Address Select
DWE_N	SSTL18	DO	Write Enable
DLDQS	SSTL18	DB	DQ[7:0] Data Strobe (Differential Pair)
DLDQS_N	SSTL18	DB	Inverse DQ[7:0] Data Strobe (Differential Pair)
DUDQS	SSTL18	DB	DQ[15:8] Data Strobe (Differential Pair)
DUDQS_N	SSTL18	DB	Inverse DQ[15:8] Data Strobe (Differential Pair)
DLDM	SSTL18	DO	DQ[7:0] Data Mask
DUDM	SSTL18	DO	DQ[15:8] Data Mask
DA[12:0]	SSTL18	DO	Address Bus
DBANK[2:0]	SSTL18	DO	Bank Address
DQ[15:0]	SSTL18	DB	Data Bus

9.3. SSTL18 Un-Terminated Output Load Example

In many applications where interconnections are short, there is no need for any termination.

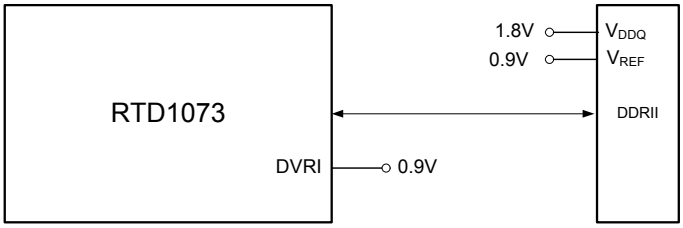


Figure 7. SSTL18 Un-Terminated Output Load Example

10. Flash Controller

The flash controller supports serial NOR flash memory and 8-bit NAND type flash memory. Each type could be configured as boot device.

10.1. Feature

- Serial NOR Flash
  - Supports up to 16MB
  - Compliant with SST/NexFlash/ATMEL/MXIC/STMicron flash memories
- NAND Flash
  - Built-in SRAM buffer to improve performance
  - Built-in 4-bit ECC mechanism to enhance data reliability
  - Supports up to 4 flash chips with interleave accessing

10.2. Serial Flash Block External Pin Description

Table 8. Serial Flash Block External Pin Description

Pin Name	IO Standard	Type	Description
SPI_CE_N	LVTTL	DO	Serial Flash Chip Select Output
SPI_WP_N	LVTTL	DO	Serial Flash Write Protect
SPI_SEL	LVTTL	DI	Select Read Command for Boot-Up 0: Op code is 0xD2 1: Op code is 0x03
SPI_SCK	LVTTL	DO	Serial Flash Clock
SPI_SI	LVTTL	DO	Serial Flash Data Input
SPI_SO	LVTTL	DI	Serial Flash Data Output
S_FLASH	LVTTL	DI	Select Serial Flash 1: Serial
N_FLASH	LVTTL	DI	Select NAND/NOR Flash 1: NAND

10.3. NAND Flash Block External Pin Description

Table 9. NAND Flash Block External Pin Description

Pin Name	IO Standard	Type	Description
NF_CLE	LVTTL	DO	NAND Flash Command Latch Enable
NF_ALE	LVTTL	DO	NAND Flash Address Latch Enable
NF_RD_N	LVTTL	DO	NAND Flash Read Enable
NF_WR_N	LVTTL	DO	NAND Flash Write Enable
NF_RDY	LVTTL	DI	NAND Flash Ready
NF_CE_N[1:0]	LVTTL	DO	NAND Flash Chip Enable[1:0]
NF_DD[7:0]	LVTTL	DB	NAND Flash Data[7:0]
S_FLASH	LVTTL	DI	Select Serial Flash
N_FLASH	LVTTL	DI	Select NAND/NOR Flash

10.4. Flash Type Selection

Table 10. Flash Type Selection

N_FLASH	S_FLASH	SPI_SEL	Flash Type
1	0	-	8 Bit NAND Type Flash
0	1	0	Serial NOR flash, Read Op Code = 0xD2
0	1	1	Serial NOR flash, Read Op Code = 0x03

10.5. Application Examples

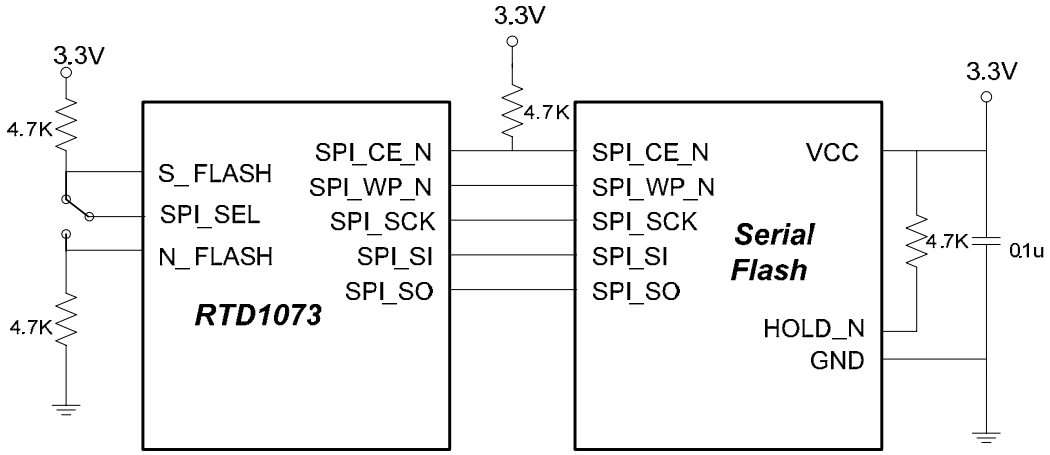


Figure 8. Typical Application of Serial Flash

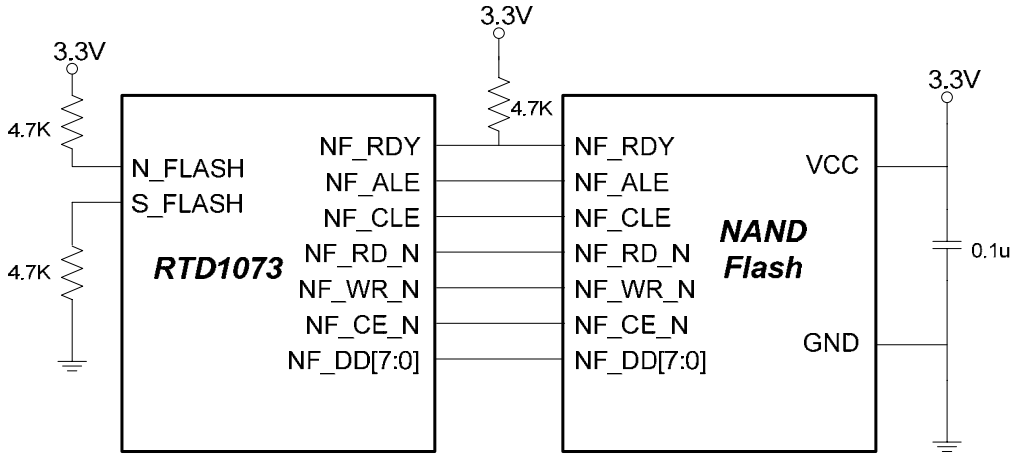


Figure 9. Typical Application of NAND Flash

11. Peripherals

11.1. General Purpose I/O

The RTD1073 provides multiple GPIO pins. Each general purpose pin can be individually configured as input or output pin via the direction configuration register. The Data output and input register can be used to control signals (high or low) when the GPIO pin is configured as output, and show the status when the GPIO pin is configured as input. When a GPIO pin is configured as input, it can also be configured as an interrupt generator (set in the interrupt enable and detection polarity register).

11.2. Universal Asynchronous Receiver and Transmitter

The RTD1073 provides two 16C550 compatible UARTs (Universal Asynchronous Receiver and Transmitter).

11.2.1. Features

- UART CH 0, 1 with 16-byte FIFO
- Programmable character properties, such as number of data bits per character (5-8), optional parity bit (with odd or even select) and number of stop bits (1, 1.5, or 2)
- Interrupt output signal occurs whenever one of the several prioritized interrupt types are enabled and active
- Receive Error
- Receive Data Available
- Character Timeout
- Transmitter Holding Register Empty at or below threshold

11.2.2. UART Block External Pin Description

Table 11. UART Block External Pin Description

Pin Name	IO Standard	Type	Description
UART_RX0	LVTTL	DI	UART 0 Receive Data Input
UART_TX0	LVTTL	DO	UART 0 Transmit Data Output
UART_RX1	LVTTL	DI	UART 1 Receive Data Input
UART_TX1	LVTTL	DO	UART 1 Transmit Data Output

11.2.3. Typical UART Application

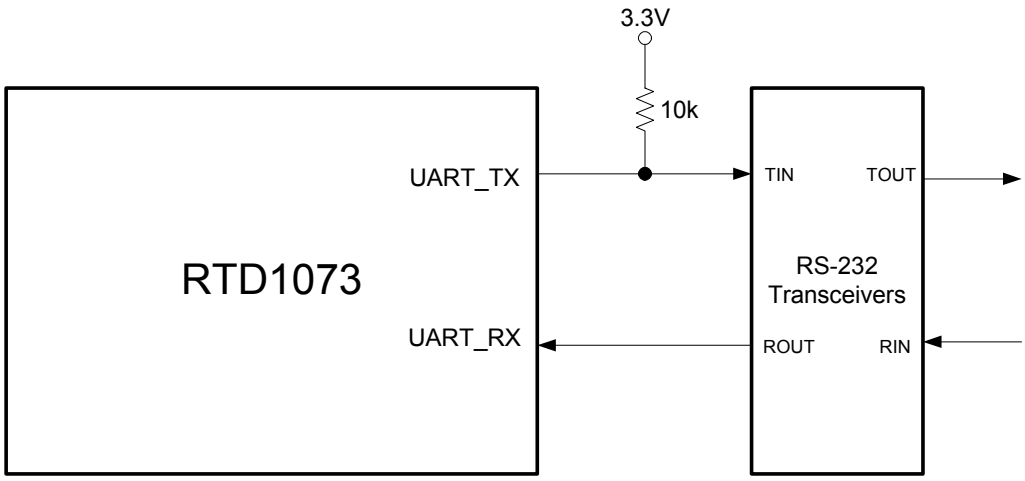


Figure 10. Typical UART Application

11.3. I²C Serial Interface

The RTD1073 can support two master/slave I²C-bus serial interfaces. A direct Serial Data Line (SDA) and Serial Clock Line (SCL) carry information between bus master and peripheral devices that are connected to the I²C-bus. The SDA and SCL lines are bi-directional.

11.3.1. Features

- Two-wire I²C serial interface
- Supports two speeds: Standard mode (100Kbps) and Fast mode (400Kbps)
- Clock synchronization
- Master or slave I²C operation
- Supports multi-Master operation (bus arbitration)
- 7-bit or 10-bit addressing
- 8 bytes transmit and receive buffers

11.3.2. I²C Block External Pin Description

Table 12. I2C Block External Pin Description

Pin Name	IO Standard	Type	Description
I2C_SCL0	LVTTL	DB	I²C Serial Clock Output
I2C_SDA0	LVTTL	DB	I²C Serial Data Signal
I2C_SCL1	LVTTL	DB	I²C Serial Clock Output
I2C_SDA1	LVTTL	DB	I²C Serial Data Signal

11.3.3. Typical I²C Application

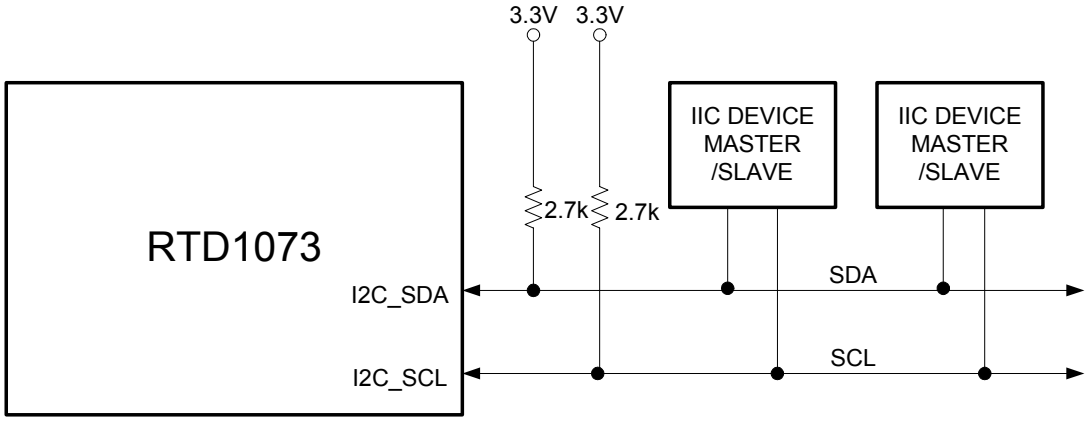


Figure 11. Typical I²C Application

11.4. Infrared Receiver Controller

The RTD1073 Infrared Receiver controller is designed for receiving commands from consumer remote controllers. It receives signals from an external IR receiver, translates signal zeros into data zeros, and accumulates data bits that conform to the register setting requirements and buffers.

11.4.1. Features

- IR channel with 2 layers of 32-bit FIFO
- Supports length-coding protocol
- Supports phase-coding protocol
- Supports phase-width modulation
- Supports phase-distance modulation
- Address and command length up to 32 bits
- Supports RAW mode for software decode remote signal

11.4.2. IR Block External Pin Description

Table 13. IR Block External Pin Description

Pin Name	IO Standard	Type	Description
IR_IN	LVTTL	DI	Infrared Input from IR Receiver, 5V Tolerant

11.4.3. Typical IR Application

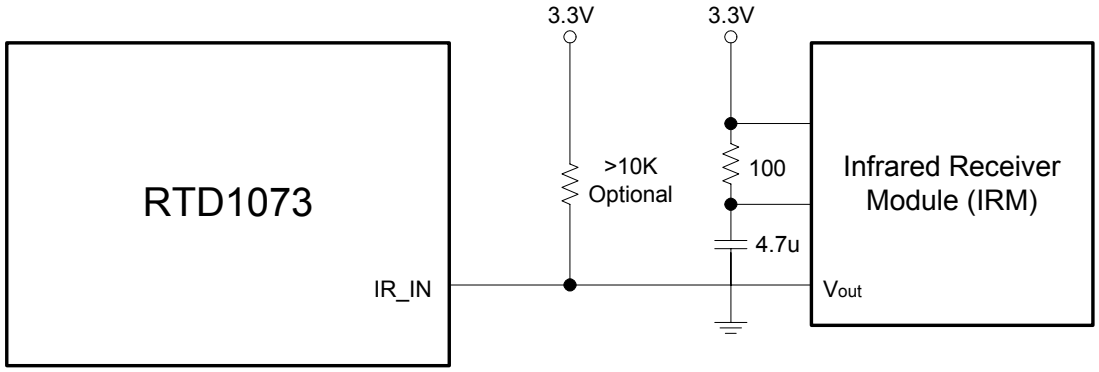


Figure 12. Typical IR Application

11.4.4. Verified Protocol

- NEC Protocol
  - Address and command are transmitted twice for reliability
  - Pulse distance modulation
  - Carrier frequency of 38kHz
  - Bit time of 1.12ms or 2.25ms
- Sony SIRC Protocol
  - Pulse width modulation
  - Carrier frequency of 40kHz
  - Bit time of 1.2ms or 0.6ms
- Philips RC-5 Protocol
  - Bi-phase coding
  - Carrier frequency of 36kHz
  - Constant bit time of 1.8ms
- Philips RC-6A Protocol (Mode 0 Only)
  - Bi-phase coding
  - Carrier frequency of 36kHz
  - Constant bit time of 888µs (except trailer bit)
- Sharp Protocol
  - Pulse distance modulation
  - Carrier frequency of 38kHz
  - Bit time of 1ms or 2ms

11.5. Timer Control

The RTD1073 provides three 32-bit timers, a 90kHz timer, and a watchdog timer. The 32-bit timer and watchdog timer count at a fixed 27MHz rate. The 90kHz timer counts at 90kHz. The 32-bit timer can be configured to timer mode or counter mode. Counter mode means the timer only times-out once. Hardware will automatically disable timer interrupts after a time-out in counter mode. Software must enable the timer interrupt and set the target value for the next usage.

11.5.1. Features

- Three sets of 32-bit timer hardware
- One 90kHz timer
- One watchdog timer
- 32-bit timer hardware can be configured to timer or counter mode
- Supports timer/counter pulse

11.6. Real Time Clock

The Real Time Clock (RTC) can be operated by the backup battery while the system power is off. The RTC data includes the time by half second, minute, hour, and date. The RTC works with an external 32.768kHz crystal and also can perform an alarm function.

11.6.1. Features

- Accepts 32.768kHz clock input
- Hex number data: Half-second, minute, hour, and date
- Programmable enable/disable half-second, minute, hour, date, and alarm interrupt
- Alarm function for system memory record
- RTC accuracy: 20ppm (under 60 second within one month)
- Operating voltage: 1.0V up to 3.3V
- Low power consumption. Keeps correct time/data for up to 48 hours with a 0.022F gold cap
- Supports reset function

11.6.2. RTC Block External Pin Description

Table 14. RTC Block External Pin Description

Pin Name	IO Standard	Type	Description
RTC_XIN	Analog	AI	Real-Time Clock 32.768kHz
RTC_XOUT	Analog	AO	Real-Time Clock 32.768kHz
RTC_VDD	Power	PWR	Power for Real Time Clock

11.6.3. Typical RTC Application

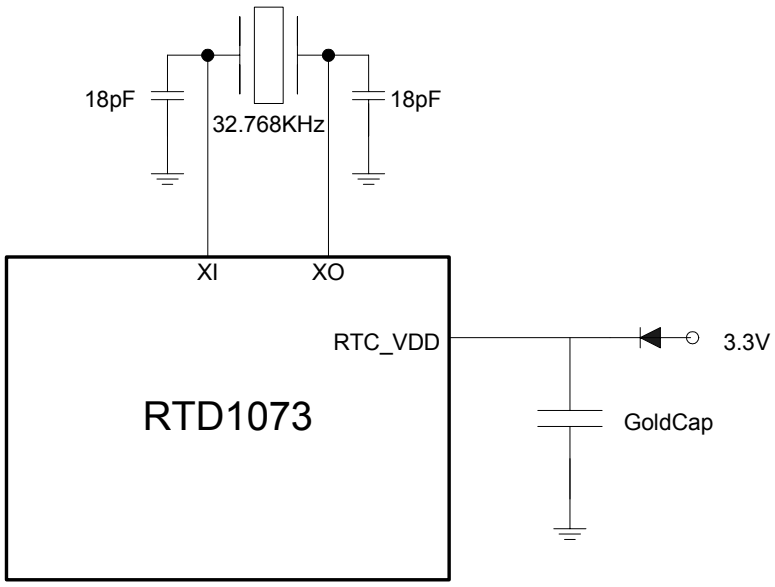


Figure 13. Typical RTC Application

11.7. Vacuum Fluorescent Display Interface

The RTD1073 provides a flexible serial interface to easily integrate with various VFD (Vacuum Fluorescent Display) controllers currently available in the market.

11.7.1. Features

- Supports general VFD (Vacuum Fluorescent Display) controller function via serial interface
- Supports key-scan function and maximum 48 keypad

11.7.2. VFD Block External Pin Description

Table 15. VFD Block External Pin Description

Pin Name	IO Standard	Type	Description
VFD_CLK	LVTTL	DO	VFD Clock, Open-Drain
VFD_CS_N	LVTTL	DO	Data Enable, Open-Drain
VFD_D	LVTTL	DB	Serial Data Input/Output, Open-Drain, 5V Tolerant

In Figure 14, all data transfer is related to the rising/falling of VFD_CLK. The LSB data bit is transferred first. The VFD_D outputs serial data at the falling edge of the clock to ensure the external VFD controller can latch the data at the rising edge of the clock. For data from the external VFD controller, VFD_D is sampled at the rising edge of the clock. The VFD clock period could be set to either 1.037µs or 2µs.

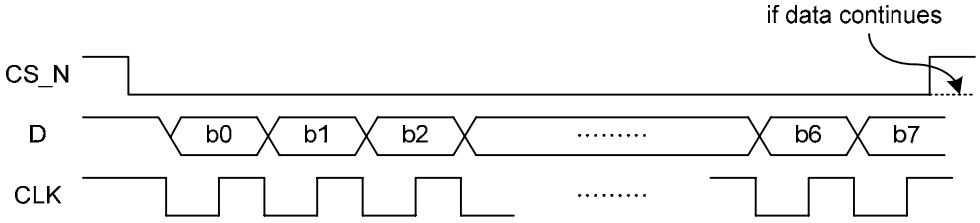


Figure 14. VFD Serial Interface Timing

11.7.3. Typical VFD Application (PT6311)

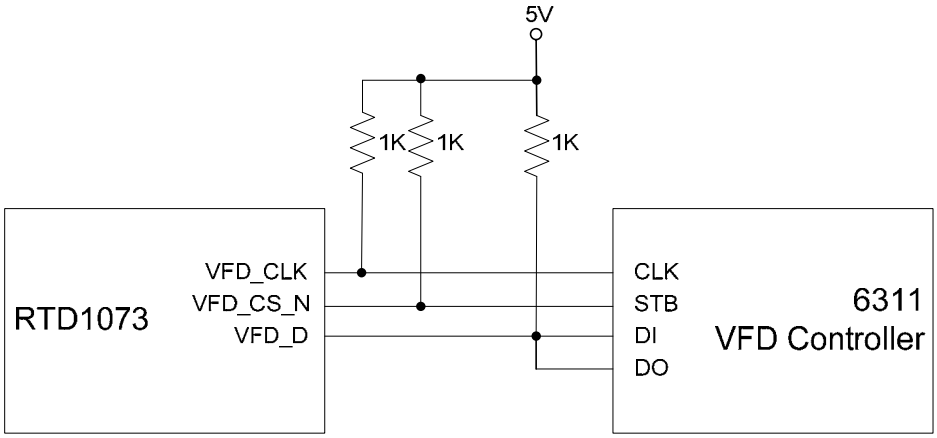


Figure 15. Typical VFD Application (PT6311)

12. TV Encoder

The TV encoder block encodes digital CR-Y-CB video data (4:2:2) to multiple standard TV signals, such as NTSC, PAL CVBS, and component YUV or RGB output signals. Four 12-bit on-chip DACs provide one composite video output, and three RGB or YPbPr component outputs. The Video output can be formatted to compatible with NTSC (M, J, 4.43), PAL (B, D, G, H, I, M, N, NC, 60), 525p, 625p, 720p, 1080i, and 1080p.

The video encoder also supports Wide-Screen Signaling (WSS), Copy Generation Management System (CGMS), and Closed Caption (CC).

12.1. Features

- Four on-chip Digital-to-Analog Converters (DACs) with 12-bit resolution for composite output (CVBS), and YPbPr or RGB component output
- Video encoding supports multi-composite format that includes NTSC[M, J, 4.43] and PAL [B, D, G, H, I, M, N, NC, 60]
- Multi-format component supports interlaced YPbPr or RGB (525i/59.94Hz and 625i/50Hz) and progressive YPbPr (525p/59.94Hz and 625p/50Hz) output
- Simultaneous composite and YPbPr outputs
- Supports HDTV YPbPr output (includes 1280×720 progressive and 1920×1080 interlaced)
- VBI encoding supports Closed Caption (CC) encoding, Wide-Screen Signaling (WSS), Video Programming System (VPS), Teletext B for PAL, and Copy Generation Management System (CGMS-A) for NTSC, 525p, 720p, 1080i, and 1080p

12.2. TV Encoder Analog Output Interface

Table 16. TV Encoder Analog Output Interface

Pin Name	IO Standard	Type	Description
VO_CVBS	Analog	AO	Analog Composite
VO_CY	Analog	AO	Component Analog Video Green or Luminance
VO_CPb	Analog	AO	Component Analog Video Blue or Pb
VO_CPr	Analog	AO	Component Analog Video Red or Pr

12.3. TV Encoder Application Examples

The RTD1073 incorporates an enhanced video encoder with four 12-bit video DACs that drive double terminated 75Ω directly without external buffering. Figure 16 shows the video DAC output circuits. Each output should connect to ground via a 75Ω resistor.

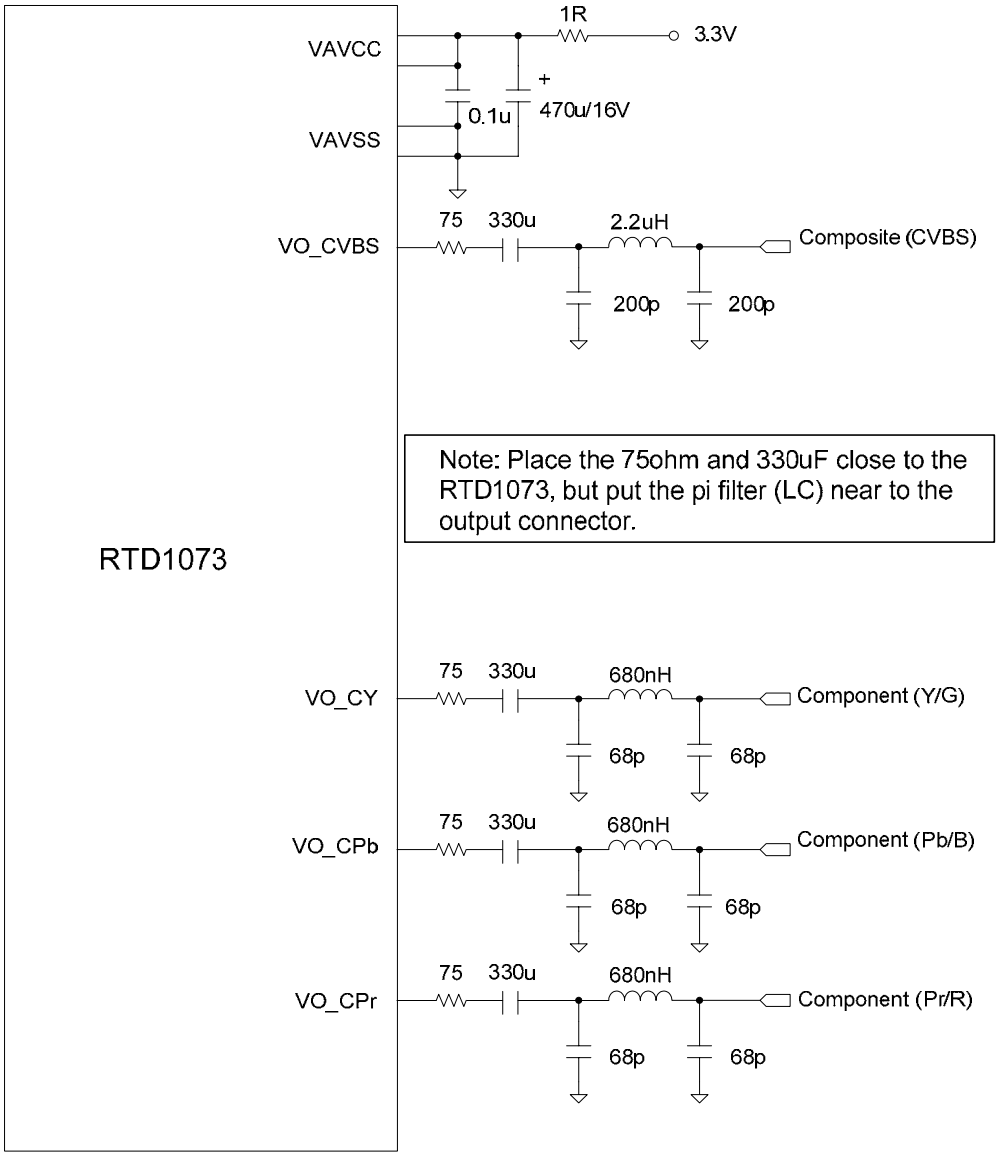


Figure 16. Typical TV Encoder (Analog) Application Circuit

13. HDMI

The RTD1073 incorporates a High Definition Multimedia Interface (HDMI) transmitter, a full-function, single-link transmitter with high-bandwidth digital content protection (HDCP), and transmits studio-quality video/audio to any HDMI/DVI/HDCP-enabled digital receiver. This module is fully compliant with the HDMI 1.3, DVI 1.0, and HDCP 1.1 specifications. The RTD1073 HDMI transmitter can also carry control and status information.

13.1. Features

- HDMI 1.3, HDCP 1.1, and DVI 1.0 compliant transmitter
  - Video Support
    - Standard-definition video format timing:
      1440 x 480i@59.94/60Hz, 1440 x 576i@50Hz, 720 x 480p@59.94/60Hz, 720 x 576p@50Hz
    - High-definition video format timing:
      1280 x 720p@59.94/60Hz, 1280 x 720p@50Hz, 1920 x 1080i@59.94/60Hz, 1920 x 1080i@50Hz, 1920 x 1080p@60Hz, 1920 x 1080p@50Hz
  - Audio Support
    - Audio sample rate: 32~192k
    - Sample size: 16~24 bit
    - Up to 8-channel
    - Supports PCM, Dolby Digital, DTS digital audio transmission
    - IEC60958 and IEC61937 compatible
- Master I^2C interface for DDC connection
- Supports Consumer Electronics Control (CEC)

13.2. HDMI Block External Pin Description

Table 17. HDMI Block External Pin Description

Pin Name	IO Standard	I/O	Description
TXC-	TMDS	AO	HDMI Output Clock Pair
TXC+	TMDS	AO	HDMI Output Clock Pair
TX0-	TMDS	AO	HDMI Output Data Pair 0
TX0+	TMDS	AO	HDMI Output Data Pair 0
TX1-	TMDS	AO	HDMI Output Data Pair 1
TX1+	TMDS	AO	HDMI Output Data Pair 1
TX2-	TMDS	AO	HDMI Output Data Pair 2
TX2+	TMDS	AO	HDMI Output Data Pair 2
CEC	Analog	AB	HDMI Consumer Electronics Control
HPD	LVTTL	DI	General Purpose I/O, for HDMI Hot Plug In

13.3. Typical HDMI Transmitter Application Circuit

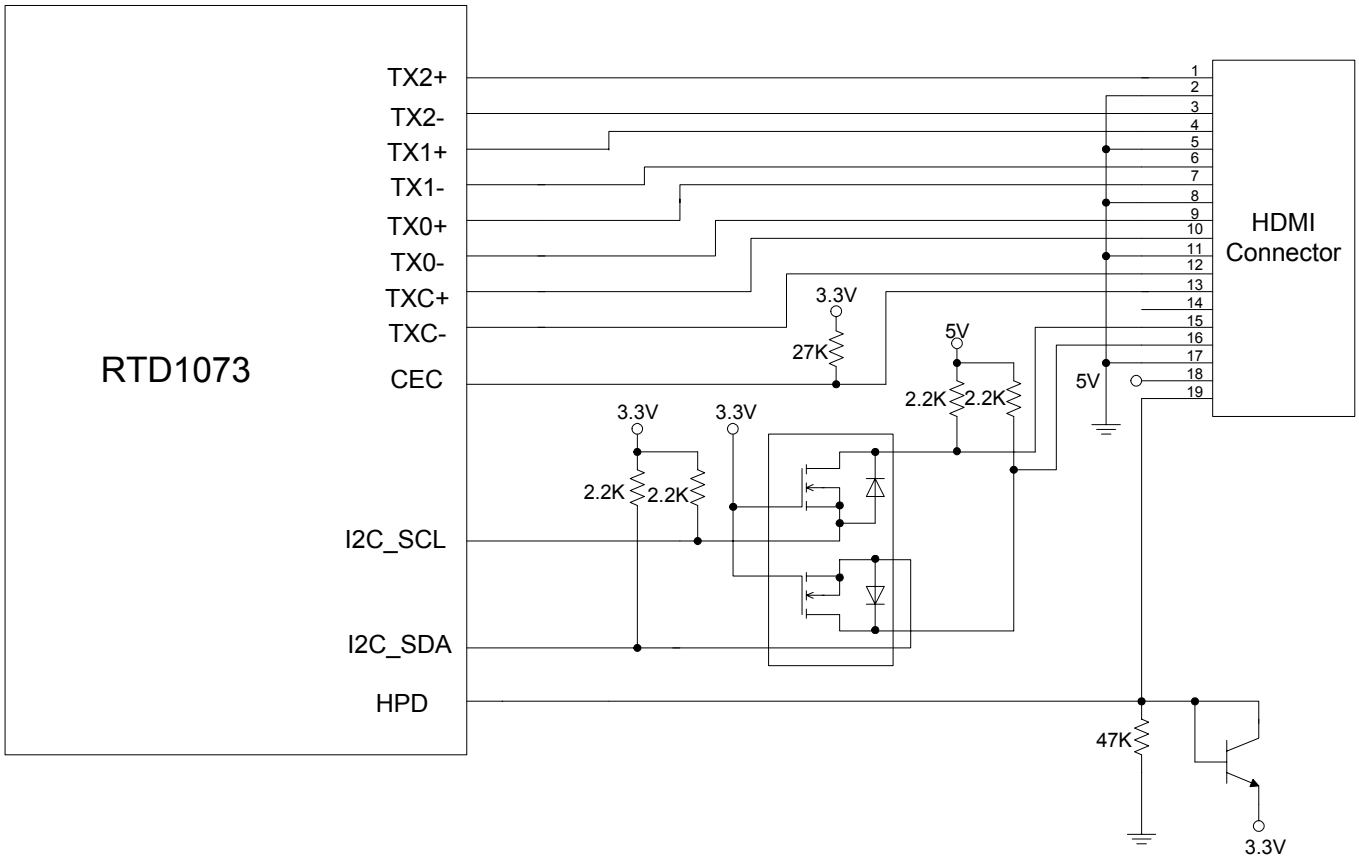


Figure 17. Typical HDMI Transmitter Application Circuit

14. Audio Out Interface

The audio Out interface transfers audio PCM data or non-PCM bit-stream data between the Audio DAC and system RAM through an internal data bus (D-bus). Two digital audio IO interfaces, I^2S and SPDIF, are supported.

For HDMI output, the RTD1073's HDMI interface can send the PCM data from Audio Out to the HDMI Tx module.

14.1. Features

- Dolby Digital Consumer Decoder (2CH)
- Dolby Digital Prologic II
- Dolby Digital Plus
- Dolby Virtual Surround
- Dolby Headphone
- MLP/Dolby Lossless
- DTS (2CH)
- DTS HD
- DTS LBR
- WMA (2CH)
- WMA Pro
- MPEG I Layer 1, 2, 3 (2CH)
- MPEG II Layer 1, 2
- MP3 Pro
- MPEG4 HE AACv2
- AAC
- OGG
- RA1/RA-cook/RA-lossless
- LPCM
- CDDA
- Post Processing
    - SRS
    - Sound Field Effect
    - Equalizer
    - Depop, resampling, fade-in, fade-out

14.2. Audio External Signal Descriptions

AO_MCLK and AO_BCLK are the reference clock signals related to the output sampling rate.

AO_LRCK is used as the Word Select line to identify the signal source.

Figure 18 shows the I²S audio-out configuration. The RTD1073 supports master mode only, meaning AO_MCLK/AO_BCLK/AO_LRCK are from the RTD1073 to an external DAC.

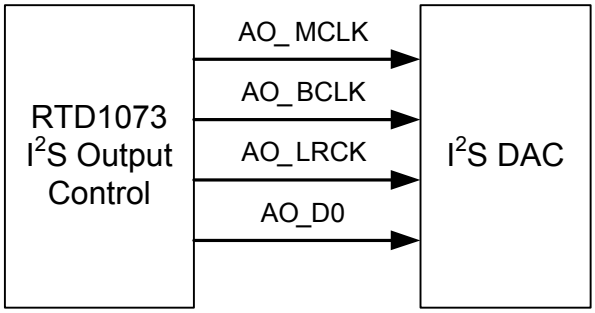


Figure 18. I²S Audio-Out Interface Configuration

Table 18. Audio Block External Pin Description

Pin Name	IO Standard	Type	Description
AO_MCLK	LVTTL	DO	Main Clock Output to DAC
AO_BCLK	LVTTL	DO	I²S Bit Clock Output to DAC
AO_LRCK	LVTTL	DO	I²S Word Select Clock Output to DAC
AO_D0	LVTTL	DO	I²S Serial Data Output for Left & Right Channels
AO_SPDIF	LVTTL	DO	IEC958 (SPDIF) Output

14.3. I²S Application Example Diagram

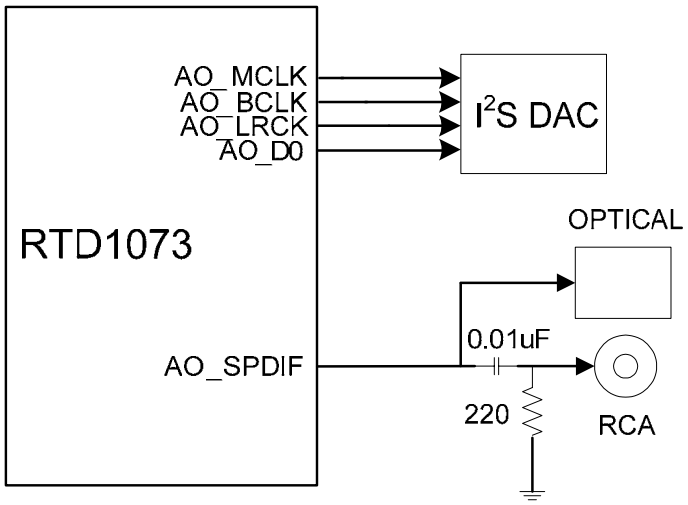


Figure 19. I²S Application Example Diagram

15. Ethernet Controller

The Realtek RTD1073 integrates a Fast Ethernet MAC, PHY, and transceiver that provide full compliance with IEEE802.3u 100Base-T specifications and IEEE802.3x Full Duplex Flow Control.

15.1. Features

- 10Mbps and 100Mbps operation
- Supports Full/Half duplex operation
- Supports descriptor-based buffer management
- Supports Tx priority queue
- Supports Auto-negotiation operation
- Supports Full Duplex Flow Control
- Supports polarity correction
- Crossover Detection & Auto-Correction

15.2. Ethernet Block External Pin Description

Table 19. Ethernet Block External Pin Description

Pin Name	IO Standard	Type	Description
TXP TXN	Analog	AO AO	Transmit Output Differential Output Pair Shared by 100Base-TX and 10Base-T Modes
RXP RXN	Analog	AI AI	Receive Input Differential Receive Input Pair Shared by 100Base-Tx and 10Base-T Modes

15.3. Typical Ethernet Application

To minimize the BOM cost, the RTD1073 has built-in 50ohm termination on each differential signal. There is no extra component needed.

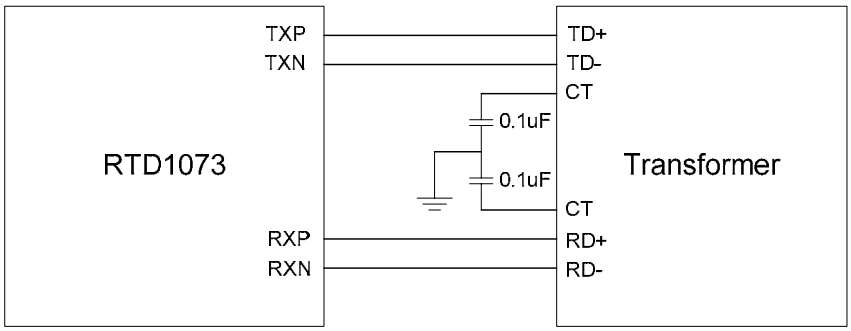


Figure 20. Typical Ethernet Application

16. USB Host/Device Controller

The RTD1073 complies with the USB2.0 standards, with operation up to 480Mbps. Two ports are built in to this chip, a downstream port and a downstream/upstream port. Each port is capable of operating at high-/full-/low-speed signaling.

16.1. Features

- Complies with EHCI and OHCI specification and with the USB2.0 specification
- EHCI compliant host for High-Speed
- OHCI compliant host for Full-/Low-Speed
- High-/Full-/Low Speed device capability
- Build-in termination resistor to reduce system cost
- Supports power management for downstream port devices

16.2. USB Block External Pin Description

Table 20. USB Block External Pin Description

Pin Name	IO Standard	Type	Description
USB0_DP	USB	AB	USB 0 D+ Signal
USB0_DM	USB	AB	USB 0 D- Signal
USB0_OverCur_FLAG	LVTTL	DI	USB 0 Over-Current Detect
USB1_DP	USB	AB	USB 1 D+ Signal
USB1_DM	USB	AB	USB 1 D- Signal
USB1_OverCur_FLAG /USB1_VBUS	LVTTL	DI	USB 1 In Host Mode: Over-Current Detect In Device Mode: VBUS-In Detect

High-speed operation supports signaling at 480Mbps. To achieve reliable signaling at this rate, the cable is terminated at each end with a resistor from each wire to ground. The value of the resistor (on each wire) is nominally set to 1/2 the specified differential impedance of the cable, or 45Ω. This presents a differential termination of 90Ω.

16.3. Application Examples

The USB_OverCur_FLAG in host mode is an active-low signal coming from an external power management chip. When an over-current event occurs, the external power management chip will shutdown the VBUS power and assert the USB_OverCur_FLAG signal.

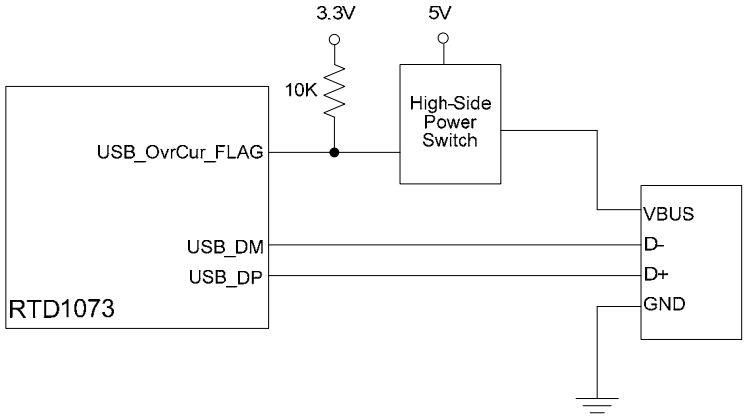


Figure 21. Typical USB Host Application with External Power Switch

As well as the external power management chip, other over-current protection devices can be applied for current limiting, e.g., Polymeric PTCs. Figure 22 shows the USB_OverCur_FLAG connected to a simple voltage divider to detect over-current events.

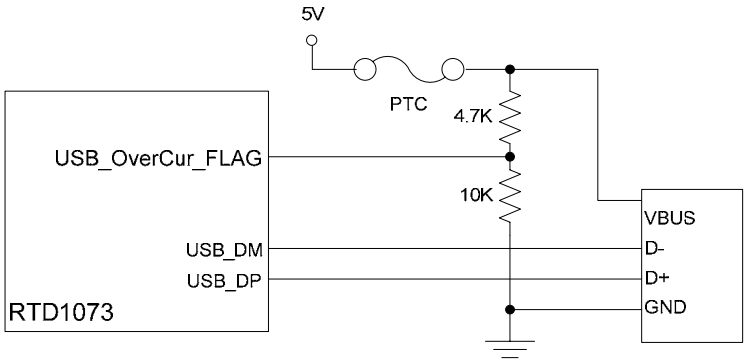


Figure 22. Typical USB Host Application with PTC

In device mode, the USB_VBUS signal indicates whether the RTD1073 is connected to a host or not.

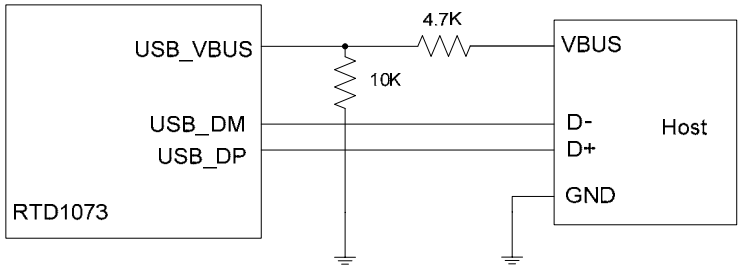


Figure 23. Typical USB Device Application

17. SATA Controller

The RTD1073 integrates a dual SATA interface with a built-in SATA PHY. On-the-fly encryption/decryption capability is provided, such as DeCSS (DVD), CPPM (DVD Audio), CPRM (DVD-R/-RW), Vidi (DVD+R/+RW), and AACS (HD-DVD/Blue-ray DVD).

17.1. Features

- The Host controller complies with the SATA 1.0a specification and is compatible with the SATA II extension specification
  - Registers are backward compatible with PATA
  - Supports 1.5Gbps and 3.0Gbps Speeds
  - Supports PIO mode
  - Supports Power Down mode
- PHY Layer (analog) function module complies with 1.0a Specification
  - Transmits a 1.5Gbps (3Gb) differential NRZ serial stream
  - Receives a 1.5Gbps (3Gb) +350/-5000ppm differential NRZ serial stream
  - Supports 5000ppm clock down spread spectrum function
  - Supports Out-of-Band signal generator and detector
  - Supports speed transition between 1.5Gbps and 3Gbps
  - Supports Low Power Mode (Partial or Slumber) at PHY Layer
  - Supports MDIO interface to configure internal PHY layer registers setting
  - Supports 32-bit/75MHz (3.0Gbps) or 32-bit/37.5MHz (1.5Gbps) parallel interface with Serial-ATA Mac Layer
- Transmits/extracts data with/without Spread Spectrum Clocking (SSC)
- Device status detection and auto speed negotiation
- Supports low power mode

17.2. SATA Block External Pin Description

Table 21. SATA Block External Pin Description

Pin Name	IO Standard	Type	Description
SATA0_HSOP	SATA	AO	First SATA TX+ Signal
SATA0_HSON	SATA	AO	First SATA TX- Signal
SATA0_HSIP	SATA	AI	First SATA RX+ Signal
SATA0_HSIN	SATA	AI	First SATA RX- Signal
SATA1_HSOP	SATA	AO	Second SATA TX+ Signal
SATA1_HSON	SATA	AO	Second SATA TX- Signal
SATA1_HSIP	SATA	AI	Second SATA RX+ Signal
SATA1_HSIN	SATA	AI	Second SATA RX- Signal

17.3. Typical SATA Application

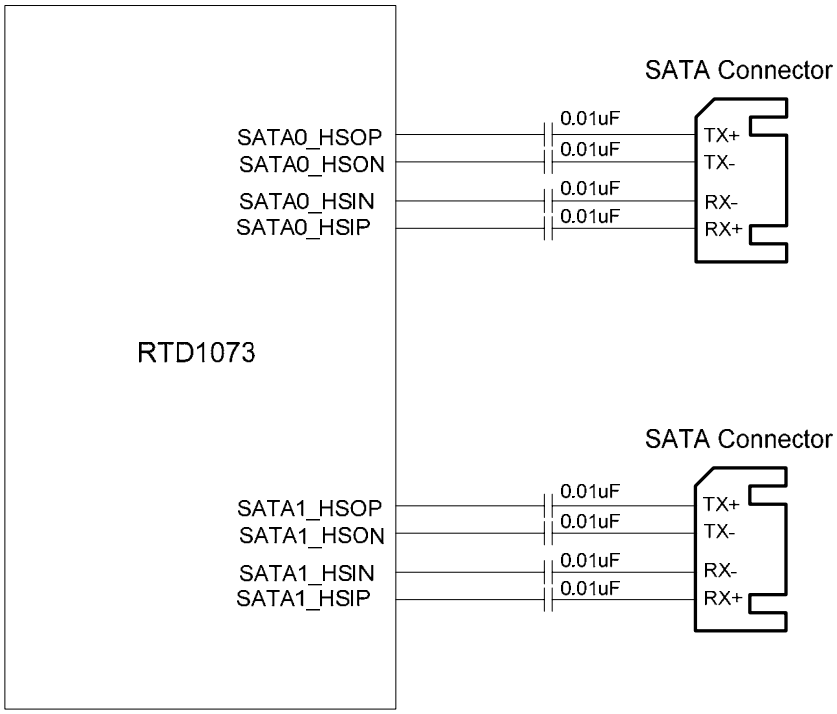
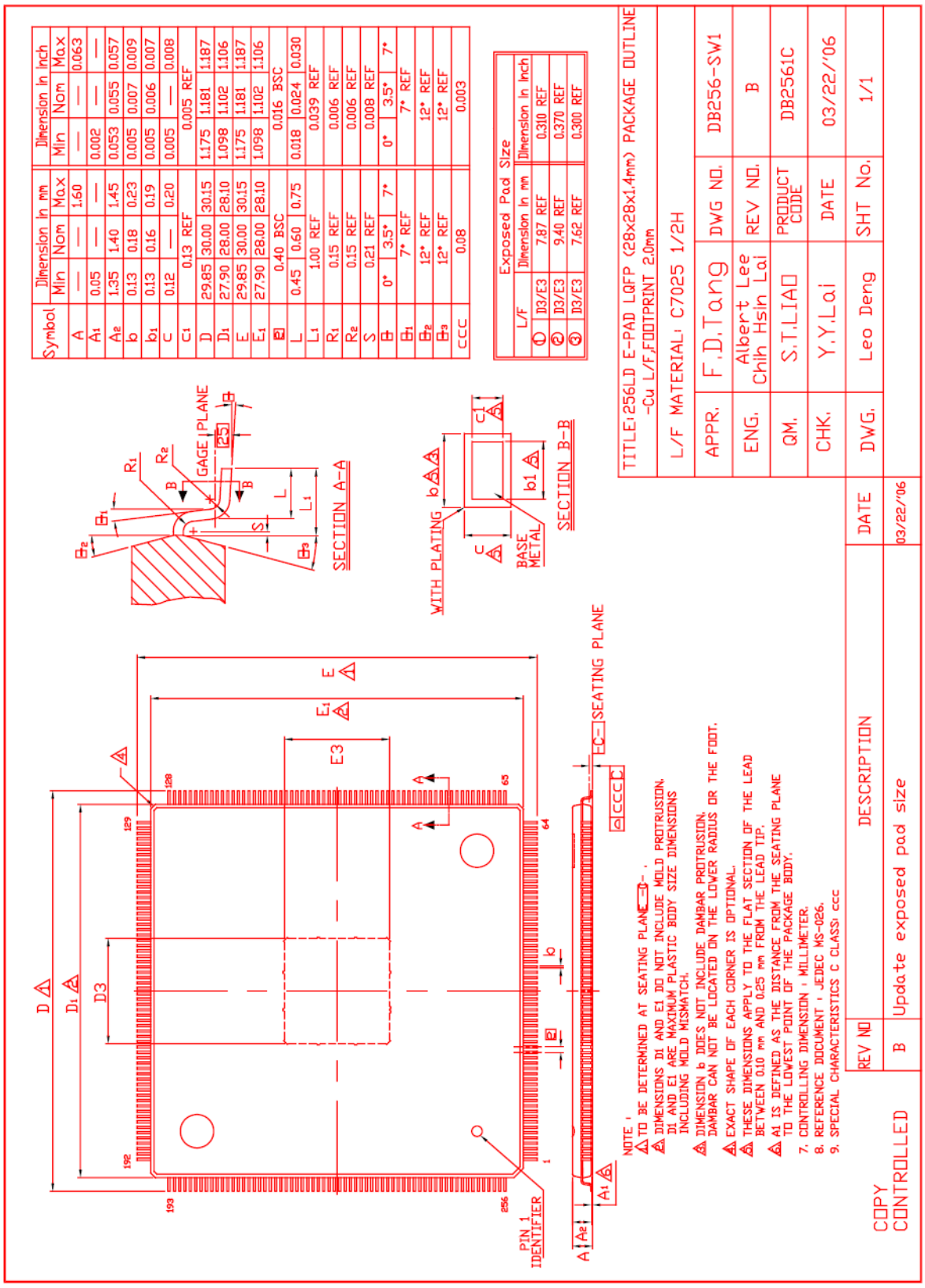


Figure 24. Typical SATA Application

18. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in Inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.12	—	0.20	0.005	—	0.008
c1	0.13 REF			0.005 REF		
D	29.85	30.00	30.15	1.175	1.181	1.187
D1	27.90	28.00	28.10	1.098	1.102	1.106
E	29.85	30.00	30.15	1.175	1.181	1.187
E1	27.90	28.00	28.10	1.098	1.102	1.106
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.15 REF			0.006 REF		
R2	0.15 REF			0.006 REF		
S	0.21 REF			0.008 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	7° REF			7° REF		
θ2	12° REF			12° REF		
θ3	12° REF			12° REF		
ccc	0.08			0.003		

Exposed Pad Size		
L/F	Dimension in mm	Dimension in Inch
① D3/E3	7.87 REF	0.310 REF
② D3/E3	9.40 REF	0.370 REF
③ D3/E3	7.62 REF	0.300 REF

18.1. Soldering Reflow Profile

The reflow profile is for MSL classification only, not the recommendation for SMT process. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 22.

Table 22. Classification Reflow Profile

Profile Feature	Green Assembly
Average Ramp-Up Rate (T_L to T_P)	3°C/second max
Preheat Ts_{min} Ts_{max} t_S	 150°C min 200°C max 60~180 seconds
Time Maintained Above T_L t_L	 217°C 60~150 seconds
Peak/Classification Temperature (T_P)	260°C max
Time within 5°C of Actual Peak Temperature (t_P)	20~40 seconds
Ramp-Down Rate (T_P to T_L)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

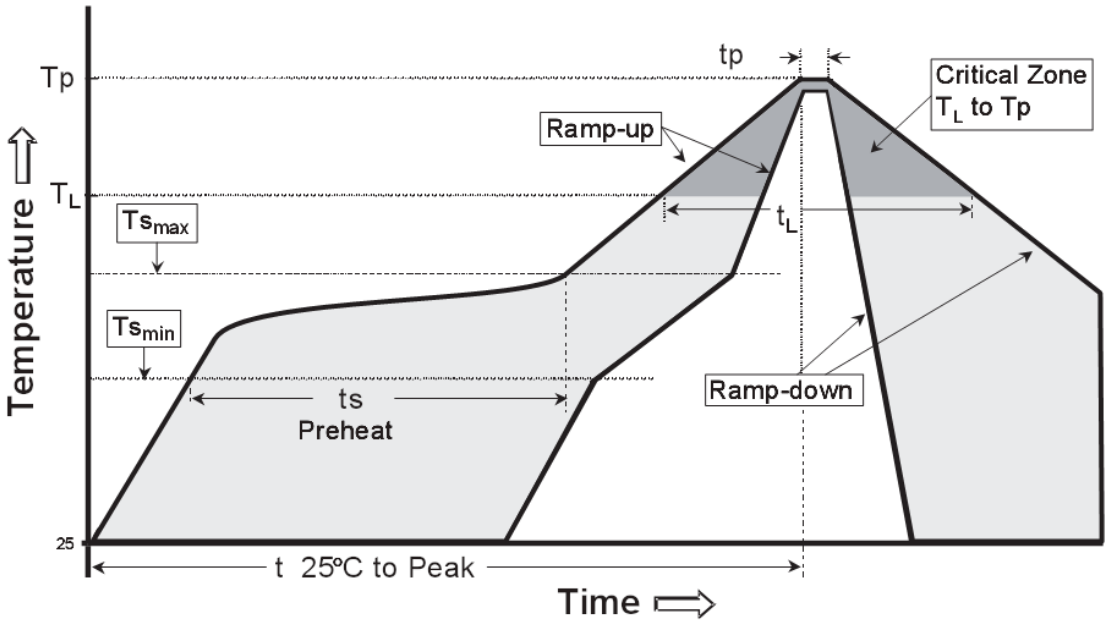


Figure 25. Soldering Temperature Profile

19. Ordering Information

Table 23. Ordering Information

Part Number	Description	Status
RTD1073DD-GR	256-Pin E-Pad LQFP & 'Green' Package. Dolby and DTS certified	Sample Release
RTD1073DA-GR	256-Pin E-Pad LQFP & 'Green' Package. Dolby certified	Sample Release

Note 1: See section 5.1 for package and version identification.
Note 2: See section 7 for licensing information.
Note 3: Only licensees certified by the original licensor(s) are eligible to purchase these products.

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