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RTL8125BG-CG
RTL8125BGS-CG

INTEGRATED 10/100/1000M/2.5G ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2019/09/03	First release.
1.1	2019/10/04	Removed 1.8V compatible input and output. Corrected minor typing errors.
1.2	2019/11/28	Revised features for 10M BASE-Te. Added note under Table 22 Power Sequence Parameters, page 32. Revised Table 25 Electrostatic Discharge Performance, page 33 (CDM ESD). Revised Table 29 DC Characteristics, page 36 (Icc). Corrected minor typing errors.
1.3	2020/01/22	Revised Table 27 Oscillator Requirements, page 35 (RMS Jitter). Corrected minor typing errors.
1.4	2020/04/20	Revised Table 11 Other Pins, page 11 (PPS_PIN). Removed Virtual Machine Queue (VMQ) data. Corrected minor typing errors.
1.5	2020/07/27	Added section 7.27 Rx High Priority Interrupt, page 30. Corrected minor typing errors.

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1. General Description

The Realtek RTL8125BG/RTL8125BGS 10/100/1000M/2.5G Ethernet controller combines a four-speed IEEE 802.3 compatible Media Access Controller (MAC) with a four-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8125BG/RTL8125BGS offers high-speed transmission over CAT 5e UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds. The RTL8125BGS provides a built-in switching regulator.

The RTL8125BG/RTL8125BGS supports the PCI Express 2.1 bus interface for host communications with power management, and is compatible with the IEEE 802.3u specification for 10/100Mbps Ethernet, the IEEE 802.3ab specification for 1000Mbps Ethernet and the IEEE 802.3bz specification for 2500Mbps Ethernet. It supports an auxiliary power auto-detect function and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8125BG/RTL8125BGS. To further reduce power consumption, the RTL8125BG/RTL8125BGS also supports PCIe L1 substate L1.1 and L1.2.

The RTL8125BG/RTL8125BGS supports ‘RealWoW!’ technology that enables remote wake-up of a sleeping PC through the Internet. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Note: The ‘RealWoW!’ service requires registration on first time use.

The RTL8125BG/RTL8125BGS supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious Wake-Up and further reduce power consumption. The RTL8125BG/RTL8125BGS can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8125BG/RTL8125BGS supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8125BG/RTL8125BGS supports IEEE 1588, IEEE 1588-2008, and IEEE 802.1AS, also known as Precision Time Protocol (PTP). IEEE 802.1AS is part of the Ethernet AVB (Audio Video Bridging) standard. PTP provides micro-second level accuracy time synchronization among multiple Ethernet devices. The RTL8125BG/RTL8125BGS implements hardware support for these standards. The RTL8125BG/RTL8125BGS supports IEEE 802.1Qav, also part of the Ethernet AVB standard. IEEE 802.1Qav is a forwarding and queuing mechanism enhancement. It provides guarantees for time-sensitive (i.e., bounded latency and delivery variation), loss-sensitive real-time audio video (AV) data traffic transmissions.

The RTL8125BG/RTL8125BGS supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az-2010 operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The RTL8125BG/RTL8125BGS is compatible with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802.1P Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN) and IEEE 802.1ad Double VLAN. The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8125BG/RTL8125BGS supports Receive-Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The maximum supported jumbo frame length of the RTL8125BG/RTL8125BGS is 16384 bytes.

The device features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8125BG/RTL8125BGS is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

Hardware

- Integrated 10M BASE-Te and 100/1000M/2.5G BASE-T 802.3 compatible transceiver
- Supports 2.5G Lite (1G data rate) mode
- Auto-Negotiation with Extended Next Page capability (XNP)
- Compatible with NBASE-T™ Alliance PHY Specification
- Supports PCI Express 2.1
- Supports pair swap/polarity/skew correction
- Configurable MDI port ordering (MDI swap) for easy PCB layout
- Crossover Detection & Auto-Correction
- Supports 1-Lane 2.5/5Gbps PCI Express Bus
- Embedded OTP memory can replace external EEPROM
- Supports hardware ECC (Error Correction Code) function
- Supports hardware CRC (Cyclic Redundancy Check) function
- Transmit/Receive on-chip buffer support
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports 25MHz Crystal / External Oscillator
- Built-in switching regulator (RTL8125BGS only)
- Generate reference clock from Crystal
- Supports power down/link down power saving/PHY disable mode
- LAN disable with GPIO pin
- Customized LEDs
- Controllable LED Blinking Frequency and Duty Cycle
- Self-Loopback diagnostic capability
- Thermal management
- 48-pin QFN 'Green' package
- Serial EEPROM
- Supports 32Mbytes External Serial Peripheral Interface (SPI) Flash
- Supports ECMA-393 ProxZzzy Standard for sleeping hosts
- Supports LTR (Latency Tolerance Reporting)
- Wake-On-LAN and 'RealWoW!' Technology (remote wake-up) support
- Supports 32-set 128-byte Wake-Up Frame pattern exact matching
- Supports Microsoft WPI (Wake Packet Indication)
- Supports PCIe L1 substate L1.1and L1.2
- Supports Rx High Priority Interrupt

IEEE

- Compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 1588v1, IEEE 1588v2, IEEE 802.1AS time synchronization
- Supports IEEE 802.1Qav credit-based shaper algorithm
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.1ad Double VLAN
- Supports IEEE 802.3az (Energy Efficient Ethernet)
- Supports IEEE 802.3bz (2.5GBase-T)
- Supports Full Duplex flow control (IEEE 802.3x)

Software Offload

- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports jumbo frame to 16K bytes
- Supports quad core Receive-Side Scaling (RSS)
- Supports Protocol Offload (ARP & NS)

Realtek Dragon Software

- Smart Auto Adjust Bandwidth Control
- Visual User Friendly UI
- Visual Network Usage Statistics
- Optimized Default Setting for Game, Browser, and Streaming Modes
- User Customized Priority Control

3. System Applications

- PCI Express 10/100/1000/2500M Ethernet on Motherboard, Notebook, or Embedded systems.

4. Function Block Diagram

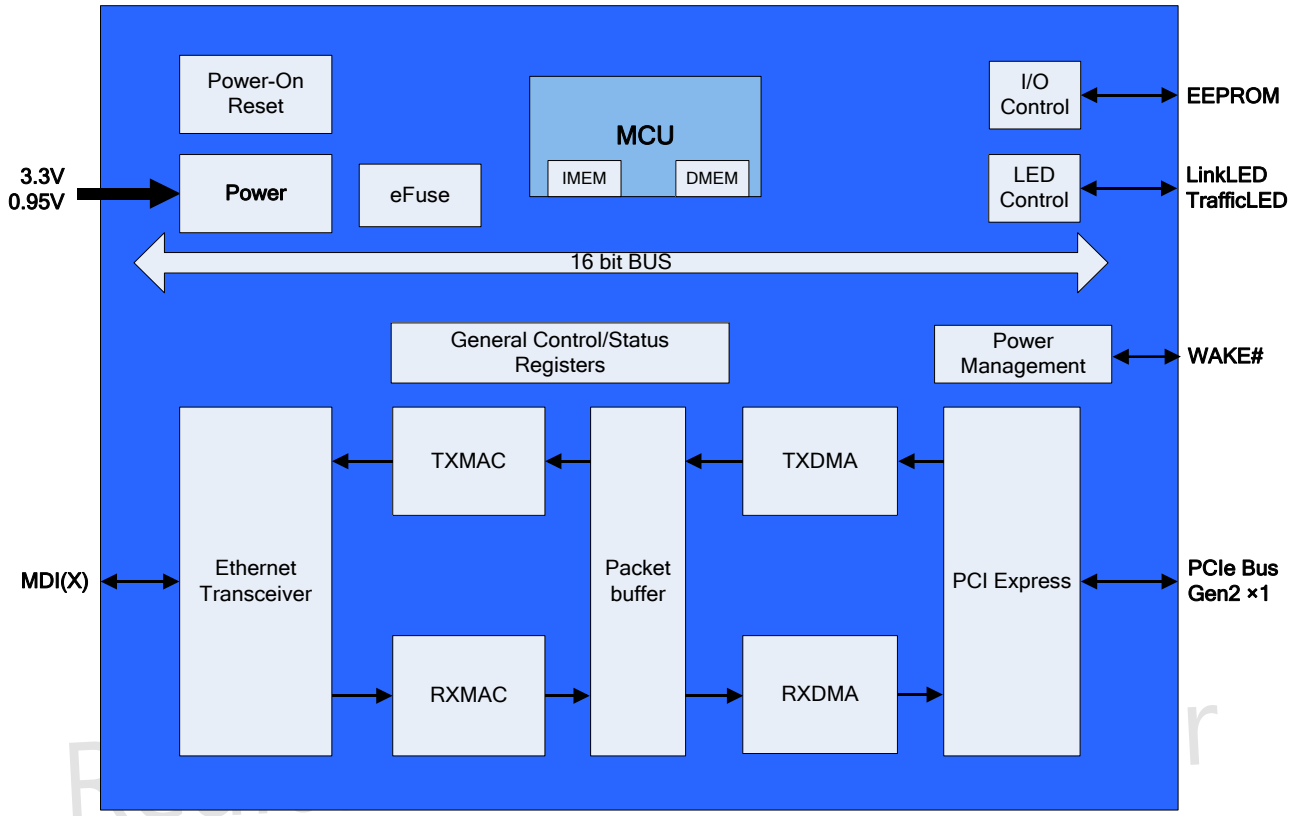


Figure 1. Function Block Diagram

5. Pin Assignments

5.1. RTL8125BG Pin Assignments

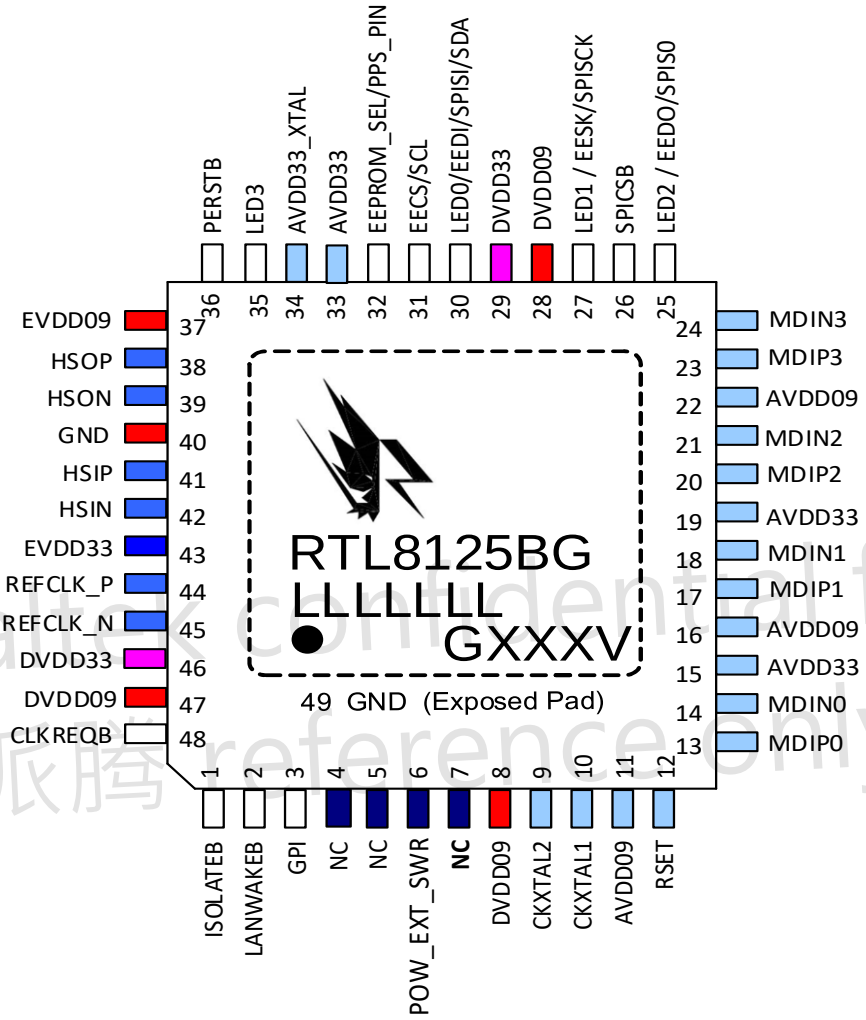


Figure 2. RTL8125BG Pin Assignments

5.2. RTL8125BG Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 2). The letter in the 'V' location indicates the IC version; a blank is used for version A.

5.3. RTL8125BGS Pin Assignments

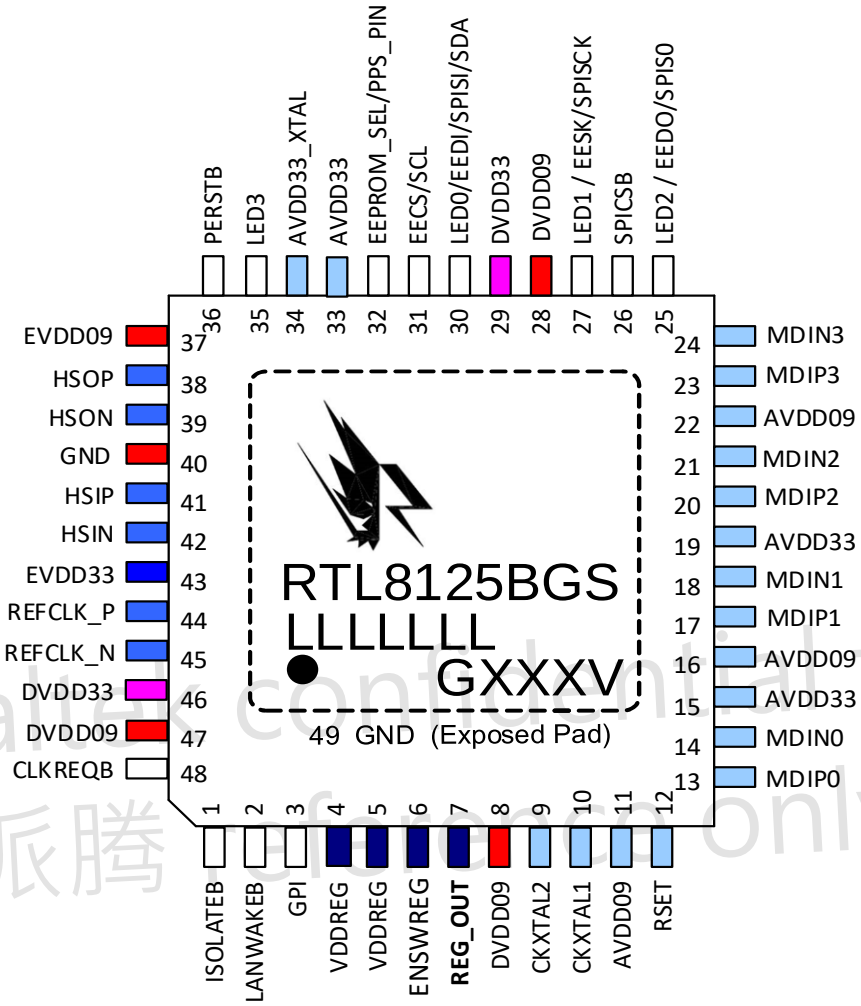


Figure 3. RTL8125BGS Pin Assignments

5.4. RTL8125BGS Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 3). The letter in the 'V' location indicates the IC version; a blank is used for version A.

6. Pin Descriptions

The signal type codes below are used in the following tables:

I:	Input	S/T/S:	Sustained Tri-State
O:	Output	O/D:	Open Drain
T/S:	Tri-State Bi-Directional Input/Output Pin	P:	Power

6.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	I/O/D	2	Power Management Event: (Open drain, active low). Used to reactivate the PCI Express slot's main power rails and reference clocks. For Strapping (internal floating, need external pull up) For normal function, this pin must be externally pulled up with a 1K~4.7K ohm resistor. If this pin is pulled low during power on reset, the RTL8125BG/RTL8125BGS will enter into test mode.
ISOLATEB	I	1	Isolate Pin: (Active Low). Used to isolate the RTL8125BG/RTL8125BGS from the PCI Express bus. The RTL8125BG/RTL8125BGS will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted. The isolate pin will follow the system state S0 to high, and S3/S4 to low.

Note 1: Power on reset after 0.95V core logic ready => min: 21ms
Note 2: Test mode is used only by Realtek.

6.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	44	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	45	
HSOP	O	38	PCI Express Transmit Differential Pair.
HSON	O	39	
HSIP	I	41	PCI Express Receive Differential Pair.
HSIN	I	42	
PERSTB	I	36	PCI Express Reset Signal: (Active Low). When the PERSTB is asserted at power-on state, the RTL8125BG/RTL8125BGS returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.

Symbol	Type	Pin No	Description
CLKREQB	I /O/D	48	Reference Clock Request Signal (Open Drain; Active Low). This signal is used by the RTL8125BG/RTL8125BGS to request starting of the PCI Express reference clock. The signal is also used by the L1.2 mechanism. In this case, CLKREQB can be asserted by either the system or RTL8125BG/RTL8125BGS to initiate a L1 exit.

6.3. Transceiver Interface

Table 3. Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	IO	13	In MDI mode, this is the first pair in 2.5G BASE-T, 1000BASE-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10BASE-Te and 100BASE-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10BASE-Te and 100BASE-TX. If MDI swap is set, this pair is BI_DD+/- in MDI mode and is BI_DC+/- in MDI crossover mode.
MDIN0	IO	14	
MDIP1	IO	17	In MDI mode, this is the second pair in 2.5G BASE-T, 1000BASE-T, i.e., the BI_DB+/- pair, and is the receive pair in 10BASE-Te and 100BASE-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10BASE-Te and 100BASE-TX. If MDI swap is set, this pair is BI_DC+/- in MDI mode and is BI_DD+/- in MDI crossover mode.
MDIN1	IO	18	
MDIP2	IO	20	In MDI mode, this is the third pair in 2.5G BASE-T, 1000BASE-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair. If MDI swap is set, this pair is BI_DB+/- in MDI mode and is BI_DA+/- in MDI crossover mode.
MDIN2	IO	21	
MDIP3	IO	23	In MDI mode, this is the fourth pair in 2.5G BASE-T, 1000BASE-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair. If MDI swap is set, this pair is BI_DA+/- in MDI mode and is BI_DB+/- in MDI crossover mode.
MDIN3	IO	24	

Note: BI_DA+/-, BI_DB+/-, BI_DC+/-, BI_DD+/- means the logical wire-pairs as described in the IEEE 802.3 standard. The MDI swap register option should be set in accordance with the ICM/XFMR pin definition.

6.4. Clock

Table 4. Clock

Symbol	Type	Pin No	Description
CKXTAL1	I	10	Input of 25MHz Clock Reference. If a 25MHz oscillator is used, connect CKXTAL1 pin to the oscillator's output.
CKXTAL2	O	9	Output of 25MHz Clock Reference Keep this pin floating if an external 25MHz oscillator drives the CKXTAL1 pin.

6.5. Regulator and Reference

Table 5. Regulator and Reference

Symbol	Type	Pin No	Description
REG_OUT	O	7	For RTL8125BGS. Built-in Switching Regulator 0.95V Output.
VDDREG	P	4,5	For RTL8125BGS. Digital 3.3V Power Supply for built-in Switching Regulator.
RSET	I	12	Reference (External resistor reference).

6.6. EEPROM

Table 6. EEPROM

Symbol	Type	Pin No	Description
EESK	I/O	27	Serial Data Clock. For Strapping (internal floating, need external pull up) For normal function, this pin must be externally pulled up with a 4.7K ohm resistor. If this pin is pulled low during power on reset, the RTL8125BG/RTL8125BGS will enter into test mode. *Note: This is a share-pin with LED1/SPISCK.*
EEDI/SDA	O/I	30	EEDI: Output to serial data input pin of EEPROM. SDA: Data interface for TWSI EEPROM. Refer to the reference schematic for strapping pin information. All strapping pins are power-on latch pins. TWSI EEPROM: Power On Latch Value High Voltage 3-wire EEPROM: Power On Latch Value Low Voltage *Note: This is a share-pin with LED0/SPISI.*
EEDO	I	25	Input from Serial Data Output Pin of EEPROM. *Note: This is a share-pin with LED2/SPISO.*
EECS/SCL	O	31	EECS: EEPROM Chip Select. SCL: Clock interface for TWSI EEPROM.
EEPROM_SEL	I	32	EEPROM 93C46/93C56/93C66 Selection. Refer to the reference schematic for strapping pin information. All strapping pins are power-on latch pins. 93C46: Power On Latch Value Low Voltage 93C56/93C66: Power On Latch Value High Voltage *Note: This is a share-pin with PPS_PIN.*

6.7. SPI (Serial Peripheral Interface) Flash

Table 7. SPI Flash

Symbol	Type	Pin No	Description
SPICSB	O	26	SPI Flash Chip Select.
SPISCK	I/O	27	SPI Flash Serial Data Clock. For Strapping (internal floating, need external pull up) For normal function, this pin must be externally pulled up with a 4.7K ohm resistor. If this pin is pulled low during power on reset, the RTL8125BG/RTL8125BGS will enter into test mode. *Note: This is a share-pin with LED1/EESK.*
SPISI	O	30	Serial Data Input. *Note: This is a share-pin with LED0/EEDI/SDA.*
SPISO	I	25	Serial Data Output. *Note: This is a share-pin with LED2/EEDO.*

6.8. LEDs

Table 8. LEDs

Symbol	Type	Pin No	Description
LED0	O	30	LED Pin. *Note: This is a share-pin with EEDI/SPISI/SDA.*
LED1	I/O	27	LED Pin. For Strapping (internal floating, need external pull up) For normal function, this pin must be externally pulled up with a 4.7K ohm resistor. If this pin is pulled low during power on reset, the RTL8125BG/RTL8125BGS will enter into test mode. *Note: This is a share-pin with EESK/SPISCK.*
LED2	O	25	LED Pin. *Note: This is a share-pin with EEDO/SPISO.*
LED3	O	35	LED Pin.

Note: See section 7.2, page 13 for more details.

6.9. Power and Ground

Table 9. Power and Ground

Symbol	Type	Pin No	Description
DVDD09	P	47,28,8	Digital Core Power 0.95V Supply.
DVDD33	P	46,29	Digital Power 3.3V Supply.
AVDD09	P	22,16,11	Analog Core Power 0.95V Supply.
AVDD33	P	15,19,33	Analog Power 3.3V Supply.
EVDD33	P	43	PCIe Power 3.3V Supply.
AVDD33_XTAL	P	34	Analog Power 3.3V Supply for XTAL.
EVDD09	P	37	PCIe Core Power 0.95V Supply.
GND	P	40	Ground.
GND	P	49	Ground (Exposed Pad (E-Pad) is Analog and Digital Ground).

Note: Refer to the latest schematic circuit for correct configuration.

6.10. GPIO

Table 10. GPIO

Symbol	Type	Pin No	Description
GPI	I /O	3	General Purpose Input / Output Pin. 1. Power Saving Feature: Output pin 2. Link OK Feature: Output pin 3. PHY Disable mode (active low): Input pin 4. LAN Disable mode (active low): Input Pin

6.11. Other Pins

Table 11. Other Pins

Symbol	Type	Pin No	Description
POW_EXT_SWR	O	6	For RTL8125BG. Enable external switch regulator to generate 0.95V power. 1: Enable 0: Disable
ENSWREG	I	6	For RTL8125BGS. Enable built-in switch regulator to generate 0.95V power. 1: Enable 0: Disable
PPS_PIN	IO	32	Pulse Per Second pin. PPS clock output / PPS as input reference clock. *Note: This is a share-pin with EEPROM_SEL.*
NC	-	4,5,7	For RTL8125BG. Not Connected Pin.

7. Functional Description

7.1. PCI Express Bus Interface

The RTL8125BG/RTL8125BGS is compatible with PCI Express Base Specification Revision 2.1, and runs at a 5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8125BG/RTL8125BGS supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal is supported.

7.1.1. PCI Express Transmitter

The RTL8125BG/RTL8125BGS's PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of two extra bits. The data code groups are passed through its serializer for packet framing. The generated 5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

7.1.2. PCI Express Receiver

The RTL8125BG/RTL8125BGS's PCI Express block receives 5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8125BG/RTL8125BGS's internal Ethernet MAC to be transmitted onto the Ethernet media.

7.2. Customizable LED Configuration

The RTL8125BG/RTL8125BGS supports customizable LED operation modes via control registers. An individual control register of each LED and a global feature control register are provided to support your own LED signals, which are described in Table 12 & Table 13.

Table 12. Customized LEDs

LEDSEL	LINK				ACT/Full	High/Low Active Control
	Link 10M	Link 100M	Link 1000M	Link 2500M		
LED 0	LED0-Bit 0	LED0-Bit 1	LED0-Bit 3	LED0-Bit 5	LED0-Bit 9	LED0-Bit 12
LED 1	LED1-Bit 0	LED1-Bit 1	LED1-Bit 3	LED1-Bit 5	LED1-Bit 9	LED1-Bit 12
LED 2	LED2-Bit 0	LED2-Bit 1	LED2-Bit 3	LED2-Bit 5	LED2-Bit 9	LED2-Bit 12
LED 3	LED3-Bit 0	LED3-Bit 1	LED3-Bit 3	LED3-Bit 5	LED3-Bit 9	LED3-Bit 12

Table 13. LED Feature Control

Feature Control	LED0-Bit 12	LED1-Bit 12	LED2-Bit 12	LED3-Bit 12	LED Option Table
0	LED0 Low Active	LED1 Low Active	LED2 Low Active	LED3 Low Active	Indicates Option 1 of Table 16 is selected
1	LED0 High Active	LED1 High Active	LED2 High Active	LED3 High Active	Indicates Option 2 of Table 16 is selected

The RTL8125BG/RTL8125BGS supports two special modes: LED OFF Mode and Fixed LED Mode. In LED OFF Mode all LED pins output become floating (power saving). The Fixed LED Mode is shown in Table 14.

Table 14. Fixed LED Mode

LED0	LED1	LED2
ACT	LINK	Full Duplex + Collision
Transmit	LINK	Receive

The normal mode is set as shown in Table 15 and Table 16.

Table 15. LED Feature Control-2

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Selected Speed LINK+ Selected Speed ACT) Option 2 (see Selected Speed LINK+ All Speed ACT)

Table 16. LED Option 1 & Option 2 Settings

Link Bit				Active Bit	Description		
10	100	1000	2500		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	0	0	LED Off		
0	0	0	0	1	-	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
0	0	0	1	0	$Link_{2500}$	-	-
0	0	0	1	1	$Link_{2500}$	Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
0	0	1	0	0	$Link_{1000}$	-	-
0	0	1	0	1	$Link_{1000}$	Act_{1000}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
0	0	1	1	0	$Link_{1000}$+$Link_{2500}$	-	-
0	0	1	1	1	$Link_{1000}$+$Link_{2500}$	Act_{1000}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
0	1	0	0	0	$Link_{100}$	-	-
0	1	0	0	1	$Link_{100}$	Act_{100}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
0	1	0	1	0	$Link_{100}$+$Link_{2500}$	-	-
0	1	0	1	1	$Link_{100}$+$Link_{2500}$	Act_{100}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
0	1	1	0	0	$Link_{100}$+$Link_{1000}$	-	-
0	1	1	0	1	$Link_{100}$+$Link_{1000}$	Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
0	1	1	1	0	$Link_{100}$+$Link_{1000}$+ $Link_{2500}$	-	-
0	1	1	1	1	$Link_{100}$+$Link_{1000}$+ $Link_{2500}$	Act_{100}+Act_{1000}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	0	0	0	0	$Link_{10}$	-	-
1	0	0	0	1	$Link_{10}$	Act_{10}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	0	0	1	0	$Link_{10}$+$Link_{2500}$	-	-
1	0	0	1	1	$Link_{10}$+$Link_{2500}$	Act_{10}+ Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	0	1	0	0	$Link_{10}$+$Link_{1000}$	-	-
1	0	1	0	1	$Link_{10}$+$Link_{1000}$	Act_{10}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	0	1	1	0	$Link_{10}$+$Link_{1000}$+ $Link_{2500}$	-	-
1	0	1	1	1	$Link_{10}$+$Link_{1000}$+ $Link_{2500}$	Act_{10}+Act_{1000}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	1	0	0	0	$Link_{10}$+$Link_{100}$	-	-
1	1	0	0	1	$Link_{10}$+$Link_{100}$	Act_{10}+Act_{100}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	1	0	1	0	$Link_{10}$+$Link_{100}$+$Lin k_{2500}$	-	-

Link Bit				Active Bit	Description		
10	100	1000	2500		Link	Option 1 LED Activity	Option 2 LED Activity
1	1	0	1	1	$Link_{10}$+$Link_{100}$+ $Link_{2500}$	Act_{10}+Act_{100}+Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	1	1	0	0	$Link_{10}$+$Link_{100}$+ $Link_{1000}$	-	-
1	1	1	0	1	$Link_{10}$+$Link_{100}$+ $Link_{1000}$	Act_{10}+Act_{100}+Act_{1000}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}
1	1	1	1	0	$Link_{10}$+$Link_{100}$+ $Link_{1000}$+$Link_{2500}$	-	-
1	1	1	1	1	$Link_{10}$+$Link_{100}$+ $Link_{1000}$+$Link_{2500}$	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}	Act_{10}+Act_{100}+Act_{1000}+ Act_{2500}

Note:
Act_{10} = LED blinking when Ethernet packets transmitted/received at 10Mbps.
Act_{100} = LED blinking when Ethernet packets transmitted/received at 100Mbps.
Act_{1000} = LED blinking when Ethernet packets transmitted/received at 1000Mbps.
Act_{2500} = LED blinking when Ethernet packets transmitted/received at 2500Mbps.
$Link_{10}$ = LED lit when Ethernet connection established at 10Mbps.
$Link_{100}$ = LED lit when Ethernet connection established at 100Mbps.
$Link_{1000}$ = LED lit when Ethernet connection established at 1000Mbps.
$Link_{2500}$ = LED lit when Ethernet connection established at 2500Mbps.

All LEDs supports low power mode in preboot or system sleep status. Table 17 describes this feature.

Table 17. LED Low Power Mode

led_lp_en_x	If non-preboot and in D3 status: 1: Led_x's behavior follows Table 16 0: Default status, LED Off
led_preboot_en_x	If preboot and in D3 status: 1: Led_x's behavior follows Table 16 0: Default status, LED Off

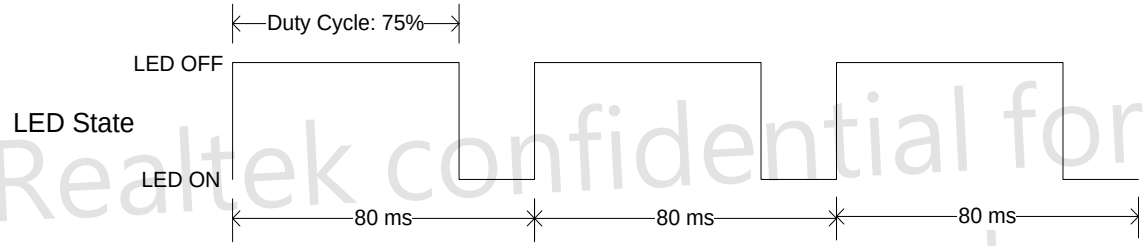
For more detailed configuration of the Customizable LED, refer to the LED App Note.

7.2.1. LED Blinking Frequency Control

The RTL8125BG/RTL8125BGS supports LED blinking frequency control to set user's LED blinking frequency and duty cycle (see Table 18). If the b_freq[1:0] set as 0x2 and the b_duty_cycle[1:0] set as 0x3, the LED blinking frequency is 80ms and the duty cycle is 75%. The LED State is shown in Figure 4.

Table 18. LED Blinking Frequency Control

Bit	RW	Description
b_freq[1:0]	RW	LED Blinking Frequency. 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
b_duty_cycle[1:0]	RW	LED Blinking Duty Cycle. 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%



Note: Assume the LED is in low active.

Figure 4. LED Blinking Frequency Example

7.3. PHY Transceiver

7.3.1. PHY Transmitter

XGMII (2500Mbps) Mode

The RTL8125BG/RTL8125BGS's PCS layer receives data bytes from the MAC through the XGMII interface and performs LDPC encoding to enhance error correction performance. After LDPC framing, each 4 bits are grouped to a PAM16 symbol though gray code mapping scheme. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT.5e cable at 200Mbaud/s through a D/A converter.

GMII (1000Mbps) Mode

The RTL8125BG/RTL8125BGS's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto the 4-pair CAT5 cable at 125Mbaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. After that, the NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

7.3.2. PHY Receiver

XGMII (2500Mbps) Mode

Received bits from the media are first passed through the on-chip sophisticated hybrid circuit to eliminate the transmitted signal interference from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, RFI cancellation, deskew, and PAM16 decoding. Each 2048-bit-wide data is passed through a LDPC decoder and is sent to the XGMII interface. The Rx MAC retrieves the packet data and sends it to the Rx Buffer Manager.

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the receive MII/GMII interface and sends it to the RX Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

7.3.3. Link Down Power Saving Mode

The RTL8125BG/RTL8125BGS implements link-down power saving; greatly cutting power consumption when the network cable is disconnected. The RTL8125BG/RTL8125BGS automatically enters link down power saving mode 3 seconds after the cable is disconnected from it. Once it enters link down power saving mode, it transmits normal link pulses on its TX pins and continues to monitor the RX pins to detect incoming signals. After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

7.3.4. Next Page

If 1000BASE-T mode is advertised, three additional Next Pages (1000BASE-T Message Page, Unformatted Page 1, and Unformatted Page 2) are automatically exchanged between the two link partners. Users can set PHY MMD7.0x10.15 to 1 to manually exchange extra Next Pages via MMD7.0x16 and MMD7.0x19 as defined in IEEE 802.3 standard.

To advertise 2.5GBASE-T capability, both link partners, sharing the same link medium, should engage in XNP (Extended Next Page) exchange. NBASE-T OUI tagged page exchange would be further needed if NBASE-T capability is to be advertised. Users can set PHY MMD7.0x0.13 to 1 to manually exchange extra Extended Next Pages via MMD7.0x16 ~MMD7.0x1B as defined in the IEEE 802.3 standard.

7.4. EEPROM Interface

Both 3-wire and TWSI EEPROM interfaces are supported. The 3-wire interface utilizes a 93C46/93C56/93C66, which is a 1K-bit/2K-bit/4K-bit, respectively, EEPROM. The EEPROM interface permits the RTL8125BG/RTL8125BGS to read from, and write data to, an external serial EEPROM device.

Values in the internal eMemory OTP or external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8125BG/RTL8125BGS will auto-load values from the eMemory OTP or EEPROM. If the EEPROM is not present and eMemory OTP auto-load is bypassed, the RTL8125BG/RTL8125BGS initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register, or using PCI VPD (Vital Product Data). The EEPROM 3-wire interface consists of EESK, EECS, EEDO, and EEDI. The TWSI interface shares SCL/SDA with EECS/EEDI.

The correct EEPROM (i.e., 93C46/93C56/93C66) must be used in order to ensure proper LAN function.

Table 19. EEPROM Interface

EEPROM	Description
EECS/SCL	93C46/93C56/93C66 Chip Select.
EESK	EEPROM Serial Data Clock.
EEDI/SDA	Output to Serial Data Input Pin of EEPROM.
EEDO	Output Data Bus.

7.5. SPI (Serial Peripheral Interface) Flash

The RTL8125BG/RTL8125BGS supports the attachment of 32MB (maximum) external Serial Peripheral Interface (SPI) Flash. The SPI flash provides 32MB bytes of serial reprogrammable flash memory.

SPI Flash is enabled by the RTL8125BG/RTL8125BGS through the Chip Select pin, and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). The SPI flash utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Table 20. SPI Flash Interface

SPI Flash	Description
SPISO	Input Data Bus.
SPISI	Output Data Bus.
SPISK	SPI Flash Serial Data Clock.
SPICSB	SPI Flash Chip Select.

7.6. Power Management

The RTL8125BG/RTL8125BGS is compatible with ACPI (Rev 1.0, 1.0b, 2.0, 3.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8125BG/RTL8125BGS can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via a PCI Express Power Management Event (PME) Message, or the LANWAKEB pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs.

When the RTL8125BG/RTL8125BGS is in power down mode (D1~D3):

- The RX state machine is stopped. The RTL8125BG/RTL8125BGS monitors the network for Wake-Up events such as a Magic Packet and Wake-Up Frame in order to wake up the system. When in power down mode, the RTL8125BG/RTL8125BGS will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the RX on-chip buffer
- The on-chip buffer status and packets that have already been received into the RX on-chip buffer before entering power down mode are held by the RTL8125BG/RTL8125BGS
- Transmission is stopped. PCI Express transactions are stopped. The TX on-chip buffer is held
- After being restored to D0 state, the RTL8125BG/RTL8125BGS transmits data that was not moved into the TX on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted

The $D3_{cold}$_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power. If aux. power is absent, the above 4 bits are all 0 in binary.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 FF, then PCI PMC = C3 FF)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 FF, then PCI PMC = 03 7E)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C3 FF (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C3 7F, then PCI PMC = C3 7F)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 7F, then PCI PMC = 03 7E)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 03 7E.

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8125BG/RTL8125BGS, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8125BG/RTL8125BGS
- The received Magic Packet does not contain a CRC error
- The RTL8125BG/RTL8125BGS driver has set up the needed registers (automatically set), and the corresponding Wake-Up method (message or LANWAKEB) can be asserted in the current power state
- The Magic Packet pattern matches, i.e., 6 * FFh + 16 * DID (Destination ID) in any part of a valid Ethernet packet

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8125BG/RTL8125BGS, e.g., a broadcast, multicast, or unicast address to the current RTL8125BG/RTL8125BGS
- The received Wake-Up Frame does not contain a CRC error
- The RTL8125BG/RTL8125BGS driver has set up the needed registers (automatically set)
- The 16-bit CRC* of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8125BG/RTL8125BGS is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet
- The 128 bytes* of the received Wake-Up Frame exactly matches the 128 bytes of the sample Wake-Up Frame pattern given by the local machine's OS

Note 1: 16-bit CRC: The RTL8125BG/RTL8125BGS supports 32-set 16-bit CRC Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial = $x^{16} + x^{12} + x^5 + 1$.

Note 2: 128-byte Wake-Up Frame: The RTL8125BG/RTL8125BGS supports 32-set 128-byte Wake-Up frames. If enabled, the 16-bit CRC Wake-Up match will be disabled.

The corresponding Wake-Up method (message or LANWAKEB) is asserted only when the following conditions are met:

- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1
- The RTL8125BG/RTL8125BGS may assert the corresponding Wake-Up method (message or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15~11) setting of the PMC register in PCI Configuration Space
- A Magic Packet, LinkUp, or Wake-Up Frame has been received
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8125BG/RTL8125BGS to stop asserting the corresponding Wake-Up method (message or LANWAKEB) (if enabled)

When the RTL8125BG/RTL8125BGS is in power down mode, e.g., D1~D3, the IO, and MEM accesses to the RTL8125BG/RTL8125BGS are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting). The setting may be changed from the EEPROM or eMemory OTP, if required.

7.7. Vital Product Data (VPD)

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8125BG/RTL8125BGS's PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56/93C66 has completed or not.

Write VPD register: (write data to the 93C46/93C56/93C66):

Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8125BG/RTL8125BGS, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.

Read VPD register: (read data from the 93C46/93C56/93C66):

Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8125BG/RTL8125BGS, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note 1: Refer to the PCI 2.3 Specifications for further information.

Note 2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.3 Specifications. VPD data is always consecutive 4-byte data starting from the VPD address specified.

Note 3: Realtek reserves offset 60h to 7Fh in EEPROM mainly for VPD data to be stored.

Note 4: The VPD function of the RTL8125BG/RTL8125BGS is designed to be able to access the full range of the 93C46/93C56/93C66 EEPROM.

7.8. Receive-Side Scaling (RSS)

The RTL8125BG/RTL8125BGS is compatible with the Network Driver Interface Specification (NDIS) 6.0 Receive-Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS allows packet receive-processing from a network adapter to be balanced across the number of available computer processors, increasing performance on multi-CPU platforms.

7.8.1. Receive-Side Scaling (RSS) Initialization

During RSS initialization, the Windows operating system will inform the RTL8125BG/RTL8125BGS that it should store the following parameters: hash function, hash type, hash bits, indirection table, BaseCPUNumber, and the secret hash key.

Hash Function

The default hash function is the Toeplitz hash function.

Hash Type

The hash types indicate which field of the packet needs to be hashed to get the hash result. There are several combinations of these fields, mainly, TCP/IPv4, IPv4, TCP/IPv6, IPv6, and IPv6 extension headers.

- TCP/IPv4 requires hash calculations over the IPv4 source address, the IPv4 destination address, the source TCP port and the destination TCP port
- IPv4 requires hash calculations over the IPv4 source address and the IPv4 destination address
- TCP/IPv6 requires hash calculations over the IPv6 source address, the IPv6 destination address, the source TCP port and the destination TCP port
- IPv6 requires hash calculations over the IPv6 source address and the IPv6 destination address
  (Note: The RTL8125BG/RTL8125BGS does not support the IPv6 extension header hash type in RSS.)

Hash Bits

Hash bits are used to index the hash result into the indirection table.

Indirection Table

The Indirection Table stores values that are added to the BaseCPUNumber to enable RSS interrupts to be restricted from some CPUs. The OS will update the Indirection Table to rebalance the load.

BaseCPUNumber

The lowest number CPU to use for RSS. BaseCPUNumber is added to the result of the indirection table lookup.

Secret Hash Key

The key used in the Toeplitz function. For different hash types, the key size is different.

7.8.2. Protocol Offload

Protocol offload is a task offload supported by Microsoft Windows 7. It maintains a network presence for a sleeping higher power host. Protocol offload prevents spurious Wake-Up and further reduces power consumption. It maintains connectivity while hosts are asleep, including receiving requests from other nodes on the network, ignoring packets, generating packets while in the sleep state (e.g., the Ethernet Controller will generate ARP responses if the same MAC and IPv4 address are provided in the configuration data), and intelligently waking up host systems. The RTL8125BG/RTL8125BGS supports the ECMA (European Computer Manufacturers Association) specification including proxy configuration and management, IPv4 ARP, IPv6 NDP, and Wake-Up packets. The RTL8125BG/RTL8125BGS also supports optional ECMA items such as QoS tagged packets and duplicate address detection.

7.8.3. RSS Operation

After the parameters are set, the RTL8125BG/RTL8125BGS will start hash calculations on each incoming packet and forward each packet to its correct queue according to the hash result. If the incoming packet is not in the hash type, it will be forwarded to the primary queue. The hash result plus the BaseCPUNumber will be indexed into the indirection table to get the correct CPU number. The RTL8125BG/RTL8125BGS uses three methods to inform the system of incoming packets: inline interrupt, MSI, and MSIX. Periodically the OS will update the indirection table to rebalance the load across the CPUs.

7.8.4. Improved RSS

Improved RSS allows a packet with specific requirements to be assigned to the specific CPU. Initialization of Improved RSS is the same as traditional RSS, except that the Indirection Table is updated by the RTL8125BG/RTL8125BGS rather than the OS.

Traditional RSS averages incoming packets to different CPUs, meaning the probability of any CPU processing the packet is equal. With 4 CPUs, each incoming packet has a 75% chance to be forwarded to an incorrect CPU. This results in re-transmission of packets to the correct destination CPU, causing wasted utilization of CPUs. The Improved RSS transmits packets to the specific CPU directly, which improves CPU efficiency.

7.9. Precision Time Protocol (PTP)

The Precision Time Protocol (PTP) is a series of IEEE 1588v1, IEEE 1588v2, and IEEE 802.1AS. These standards specify the protocol and procedures to provide high-level time synchronization on Ethernet devices for time sensitive applications, such as audio and video. The RTL8125BG/RTL8125BGS supports the standards by providing the following hardware features.

- Supports all versions of PTP standards: 1588, 1588-2008, and 802.1AS
- Layer2, UDP/IPv4, and UDP/IPv6 PTPv2 Ethernet packets supported
- Detection and time stamping of PTP packets on both TX and RX sides with resolution of 8ns
- Offset and frequency adjustable PTP clock
- One-step timestamp insertion on PTP event packets and timestamp update offload on PTP general packets
- Generation of Pulse Per Second (PPS) signal
- Hardware Time maintain Offload feature

For more detailed configuration of the PTP functions, refer to the PTP App Note.

7.10. IEEE 802.1Qav

802.1Qav is part of the Ethernet AVB (Audio Video Bridging) standard. It enhances the forwarding and queuing mechanism to meet the requirements of time-sensitive Audio/Video Streams. The RTL8125BG/RTL8125BGS implements the credit-based shaper algorithm on all TX queues. User can make bandwidth reservation on each TX queue. The hardware will control the queuing and transmitting to make sure the outgoing traffic matches the bandwidth reservation.

7.11. Double VLAN (Double Virtual Bridged Local Area Network)

The RTL8125BG/RTL8125BGS supports a mode where all received and sent packets have one VLAN tag or two VLAN tags. When a packet carries two VLAN headers, the first header is referred to as an outer VLAN and the second header as an inner VLAN. The RTL8125BG/RTL8125BGS supports tagging and de-tagging of both the outer and the inner VLAN tags. The expanded VLAN space allows the service provider to provide certain services, such as Internet access on specific VLANs for specific customers, and yet still allows the service provider to provide other types of services for their other customers on other VLANs.

7.12. Energy Efficient Ethernet (EEE)

The RTL8125BG/RTL8125BGS supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, 500Mbps, and 1000Mbps and IEEE 802.3bz-2016 EEE at 2.5G BASE-T. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

7.13. Radio Frequency Interference (RFI)

Among the many possible causes of interference when connecting two PHYs, Radio Frequency Interference (RFI) is the most common. The RTL8125BG/RTL8125BGS is equipped with RFI cancellation ability. This allows the RTL8125BG/RTL8125BGS to maintain data transmission in noisy environments and makes it immune to RFI strikes.

7.14. Fast Retrain (FR)

The RTL8125BG/RTL8125BGS supports IEEE 802.3 Fast Retrain in 2.5GBASE-T. It provides a protocol to quickly converge a Tx/Rx equalizer at both ends of the link when it is needed. If local Rx SNR is bad, or the link partner requests FR, FR is launched and it attempts to train the Tx/Rx equalizer before the link goes down.
This protocol can reduce link up/link down wait time and provide better upper layer protocols and applications. This protocol is especially useful when the RTL8125BG/RTL8125BGS is used in noisy environments or a when short time RFI happens to strike the link.

The RTL8125BG/RTL8125BGS supports CISCO Negotiated Fast Retrain, which aims for the same target as IEEE FR but extends some timing specifications to allow better weak link recovery.

7.15. Thermal Detect

When the RTL8125BG/RTL8125BGS operates in 2.5G and 2.5G Lite mode, a built-in smart thermal management can sense the temperature of the IC, regardless of the surrounding environment temperature. To prevent damage, the RTL8125BG/RTL8125BGS will depend on the current link speed to mask 2.5G or 2.5G Lite capability, and will notify the system when an over temperature event occurs. With the aid of this thermal detect mechanism, the RTL8125BG/RTL8125BGS can provide smart power management. The goal of smart power management is to give a balance between power consumption and Ethernet transceiver performance. This feature is especially useful when the RTL8125BG/RTL8125BGS is deployed in thermally constrained environments.

7.16. MDI SWAP

Different ICM (Integrated Combo Magnetics) might have opposite phy sides to the cable side definition. To accommodate this, the RTL8125BG/RTL8125BGS supports MDI swap to prevent PCB trace routing from crossing.

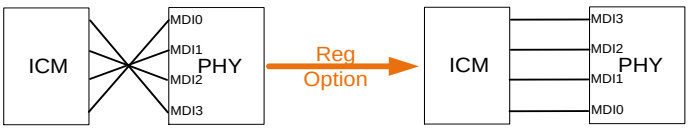


Figure 5. MDI SWAP

7.17. PHY Disable Mode

The RTL8125BG/RTL8125BGS can power down the PHY using board-level control signals.

7.18. LAN Disable Mode

The RTL8125BG/RTL8125BGS supports 'LAN Disable Mode' that can use an external signal to control whether the NIC is enabled or disabled.

7.19. Latency Tolerance Reporting (LTR)

The RTL8125BG/RTL8125BGS supports PCIe 3.0 LTR (Latency Tolerance Reporting).

The LTR mechanism enables Endpoints to report service latency requirements for Memory Reads/Writes. The CPU utilizes LTR to determine transfers from low power (C7) to high power (C0) mode. See the PCIe 3.0 specification for details.

7.20. RealWoW!' (Wake-On-WAN) Technology

The RTL8125BG/RTL8125BGS supports Realtek 'RealWoW!' technology that allows the RTL8125BG/RTL8125BGS to send keep alive packets to the Wake Server when the PC is in sleeping mode. Realtek 'RealWoW!' can pass wake-up packets through a NAT (Network Address Translation) device. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Users can login into the Wake Server via the Internet to wake the selected sleeping PC. Registration of Account information to the Wake Server is required on first time use.

7.21. Wake Packet Indication (WPI)

The RTL8125BG/RTL8125BGS supports Microsoft Wake Packet Indication (WPI) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPI helps prevent unwanted/unauthorized wake-up of a sleeping computer. Refer to the Microsoft Windows Hardware Certification Requirements for details.

Note: Wake Packet Indication (WPI) and Wake Packet Detection (WPD) are the same technology terms defined by Microsoft, and both terms mean the NIC is required to capture at least the first 128 bytes of the packet causing the network wake and generate a status indication to the operating system.

7.22. L1.1 and L1.2

The RTL8125BG/RTL8125BGS supports PCIe L1 substate L1.1 and L1.2 power management features. L1+CLKREQ# stops (or provides) the REFCLK to a device by toggling the CLKREQB pin to enter L1.1 and L1.2 states (saving more power than L1+CLKREQ# only). Table 21 shows the PCIe Port Circuit On/Off states.

Table 21. L1.1 and L1.2 PCIe Port Circuit On/Off

State	PLL	Common Mode Keeper	RX/TX
L1	On	On	Off/Idle
L1+CLKREQ#	Off	On	Off/Idle
L1.1	Off	On	Off
L1.2	Off	Off	Off

7.23. Lite Mode

7.23.1. Giga Lite

The RTL8125BG/RTL8125BGS supports Giga Lite (500M) mode that allows two link partners that both support 1000BASE-T and Giga Lite mode to transmit at 500Mbps data rate if only two pairs (AB pairs) can be detected in the CAT.5 UTP cable. This feature is a Realtek proprietary feature and it conforms to the 802.3az-2010 (EEE) specification.

7.23.2. 2.5G Lite

The RTL8125BG/RTL8125BGS supports 2.5G Lite (1000M) mode that allows two link partners that both support 2.5G BASE-T and 2.5G Lite mode to transmit at 1000Mbps data rate if only two pairs (AB pairs) can be detected in the CAT.5e UTP cable. This feature is a Realtek proprietary feature and it conforms to the 802.3az-2010 (EEE) specification.

7.24. Green Ethernet (1000M/100Mbps Mode Only)

7.24.1. Cable Length Power Saving

In 1000M/100Mbps mode the RTL8125BG/RTL8125BGS provides dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides intermediate performance with minimum power consumption.

7.25. Crossover Detection and Auto-Correction

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable. Crossover Detection & Auto-Correction Configuration eliminate the need for crossover cables between devices, such as two computers connected to each other with an Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange the MDI/MDI Crossover configuration. If the RTL8125BG/RTL8125BGS is configured to only operate in 100BASE-TX or only in 10BASE-Te mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8125BG/RTL8125BGS advertises only 100BASE-TX mode or 10BASE-Te mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1. If it is set to half duplex, then only half duplex is advertised.

2. If it is set to full duplex, then both full and half duplex are advertised.

7.26. Polarity Correction

The RTL8125BG/RTL8125BGS automatically corrects polarity errors on the receive pairs in 2.5GBASE-T, 1000BASE-T and 10BASE-Te modes. In 100BASE-TX mode polarity is irrelevant. In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. Users may manually do polarity correction via reg option if polarity is known beforehand. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-Te mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-Te link is up. The polarity becomes unlocked when the link is down.

7.27. Rx High Priority Interrupt

The RTL8125BG/RTL8125BGS supports Rx High Priority Interrupt. Rx High Priority Interrupt allows special packets to be responded to immediately. The Rx High Priority Interrupt supports 128-set TCP or UDP ports. TCP and UDP share the 128-set ports. The Rx High Priority Interrupt also supports TCP packets with the Push or URG bit enabled. As a result of this function, high priority packets have a separate Queue and can be dealt first.

8. Switching Regulator (RTL8125BGS Only)

The RTL8125BGS incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency, and lower the output voltage ripple and input overshoot. Note that the switching regulator 0.95V output pin (REG_OUT) must be connected only to DVDD09, AVDD09 and EVDD09 (do not provide this power source to other devices).

Note: Refer to the separate RTL8125BGS layout guide for details.

9. Power Sequence

9.1. Power Sequence Parameters

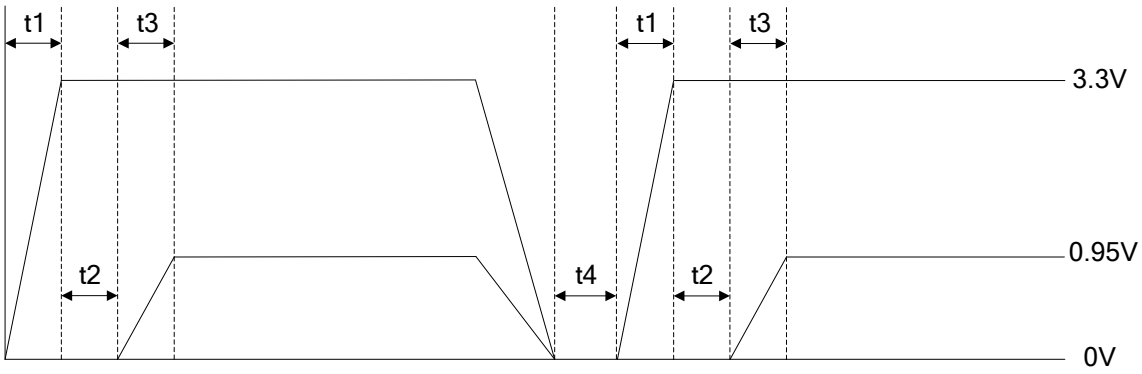


Figure 6. Power Sequence

Table 22. Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Unit
t1	3.3V Rise Time	0.5	-	10	ms
t2	SWR Enable Interval	(Note 2)	-	-	ms
t3	0.95V Rise Time for RTL8125BG	0.5	-	5	ms
	0.95V Rise Time for RTL8125BGS	-	-	5	ms
t4	On/Off Interval	50	-	-	ms

Note 1: The output DC level tolerance is ± 5% of the target voltage therefore the loosest counting of t1 would be the rising time required for power rail to output from 0V to 90% target voltage.

0.5ms < Rise Time < 10ms and monotonic ramp:

No action to take.

0.1ms < Rise Time < 0.5 ms and monotonic ramp:

If the rise time is between 0.1ms~0.5ms and the power supply is in monotonic ramp, the customer MUST ensure that there is at least three times as much margin for inrush current to the RTL8125BG(S) so as to be safely under the system's power supply OCP threshold.

For example: Assume customer supply power rise time of the RTL8125BG(S) is 0.374ms. The system power supply OCP is 9A. The inrush current of other devices is 5.64A. The inrush current to the RTL8125BG(S) must be less than 1.12A; otherwise an unanticipated system OCP may be triggered. It can be expressed in the following formula: Inrush current to the RTL8125BG(S) < (System power supply OCP - inrush current of other devices) / 3

Rise Time < 0.1 ms or non-monotonic ramp:

Under this scenario, there is risk of an unanticipated ESD trigger event, which may cause permanent damage to the RTL8125BG(S). As well as an unanticipated ESD trigger event, the power supply source with rise time < 0.1ms or > 100ms or non-monotonic ramp may possibly cause permanent damage to the RTL8125BG(S). If there is any action that involves consecutive ON/OFF toggling of the power source, the design must make sure the OFF state of all power domain reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms.

Note 2: t2 should be well controlled by the RTL8125BG(S).

10. Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 23. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
DVDD33, AVDD33, AVDD33_XTAL, EVDD33	Supply Voltage 3.3V	-0.3	3.63	V
AVDD09, DVDD09, EVDD09	Supply Voltage 0.95V	-0.2	1.05	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

10.2. Recommended Operating Conditions

Table 24. Recommended Operating Conditions

Description	Supply Voltage	Min	Typ	Max	Unit
Supply Voltage	3.3	3.14	3.3	3.46	V
	0.95	0.92	0.95	0.98	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

10.3. Electrostatic Discharge Performance

Table 25. Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: ｜3.5KV｜
MM ESD	All Pins: ｜100V｜
CDM ESD	All Pins: ｜200V｜
Latch Up	I/O Pin: 100mA Power Pin: 1.5xVDD

10.4. Crystal Requirements

A 25MHz parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to CKXTAL1 and CKXTAL2 pins. Shunt each crystal lead to ground with a 27pF capacitor.

Table 26. Crystal Requirements

Symbol	Description/Condition	Min	Typ	Max	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Tolerance (Note 1)	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	70	Ω
V_{ih}_CKXTAL	Crystal Output High Level	1.4	-	-	V
V_{il}_CKXTAL (Note 2)	Crystal Output Low Level	-	-	0.4	V
Operating Temperature Range	-	-40	-	85	°C
Package (Note 3)	-	-	SMD	-	-

Note 1: F_{ref} Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.
Note 2: Based on XTAL drive level spec to choose the appropriate resistor on CKXTAL2 pin to meet Vih and Vil requirement.
Note 3: An SMD type crystal MUST be used for the RTL8125BG/RTL8125BGS.

10.5. Oscillator Requirements

Table 27. Oscillator Requirements

Parameter	Condition	Min	Typ	Max	Unit
Frequency	-	-	25	-	MHz
Frequency Tolerance (Note 1)	Ta=0°C~70°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
RMS Jitter (Note 2)	10kHz~20MHz	-	-	2	ps
V_{ih}	-	1.4	-	-	V
V_{il}	-	-	-	0.4	V
Rise Time (10%~90%)	-	-	-	11	ns
Fall Time (10%~90%)	-	-	-	11	ns
Operating Temperature Range	-	-40	-	125	°C

Note 1: Frequency Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.

Note 2: The phase noise of 25MHz clock input should be at least that as shown in Figure 7.

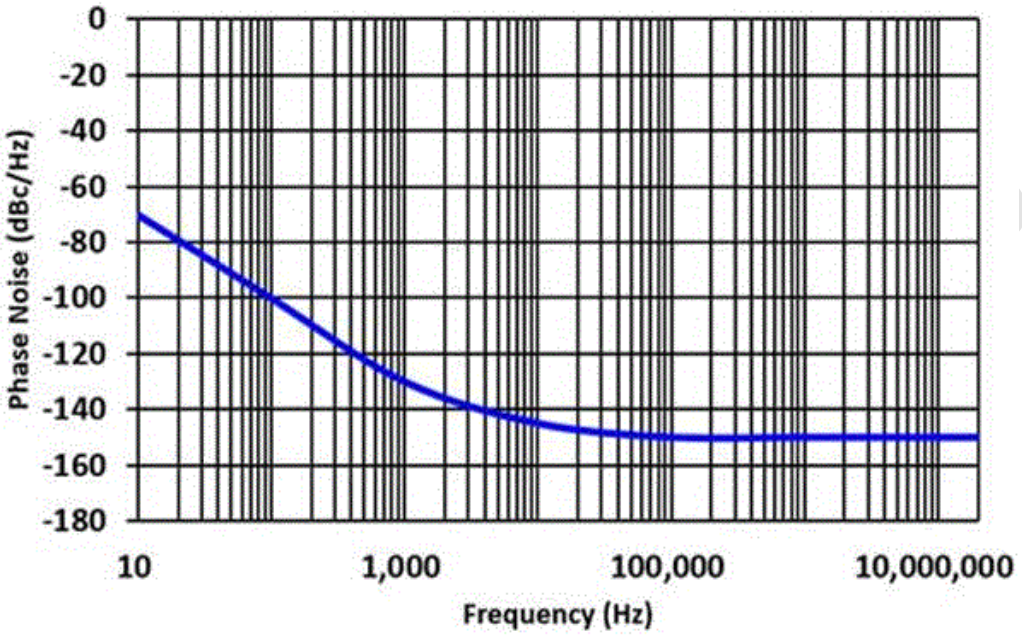


Figure 7. Phase Noise

10.6. Environmental Characteristics

Table 28. Environmental Characteristics

Parameter	Range	Units
Storage Temperature	-55 ~ +125	°C
Ambient Operating Temperature	0 ~ 70	°C
Moisture Sensitivity Level (MSL)	Level 3	N/A

10.7. DC Characteristics

Table 29. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AVDD33, DVDD33, AVDD33_XTAL EVDD33	3.3V Supply Voltage	-	3.14	3.3	3.46	V
AVDD09, DVDD09, EVDD09	0.95V Supply Voltage	-	0.92	0.95	0.98	V
Voh	Minimum High Level Output Voltage	3.3V domain	2.4	3.3	VDD33 + 0.3	V
Vol	Maximum Low Level Output Voltage	3.3V domain	-0.3	0	0.4	V
Vih	Minimum High Level Input Voltage	3.3V domain	2.0	3.3	-	V
Vil	Maximum Low Level Input Voltage	3.3V domain	-	0	0.8	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	µA
Icc	Maximum Operating Supply Current (Note 2)	3.3V domain	-	88	100	mA
		0.95V domain	-	364	650	

Note 1: Pins not mentioned above remain at 3.3V.

Note 2: The Maximum Operating Supply Current was measured under the specific conditions of 100 meter Cat5e, +5% of all power rails and Ta = 85°C. This will help the PCB designer have a better understanding of each power rail budget.

10.8. Reflow Profile Recommendations

Table 30. Reflow Profile Recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Minimum Preheat Temperature (T_{smin})	100°C	150°C
Maximum Preheat Temperature (T_{smax})	150°C	200°C
Preheat Time (t_S) from T_{smin} to T_{smax}	60~120 seconds	60~120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second max.	3°C/second max.
Liquidus Temperature (T_L)	183°C	217°C
Time (t_L) Maintained above T_L	60~150 seconds	60~150 seconds
Peak Package Body Temperature (T_p)	235°C	260°C
Time $(t_p)^2$ within 5°C of Peak T_P	20 seconds	20 seconds
Ramp-Down Rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature (T_p)	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the topside of the package, measured on the package's body surface.

Note 2: Tolerance for Tp is defined as a supplier's minimum and a user's maximum.

Note 3: Reference document: IPC/JEDEC J-STD-020D.1.

10.9. AC Characteristics

10.9.1. Serial EEPROM Interface Timing

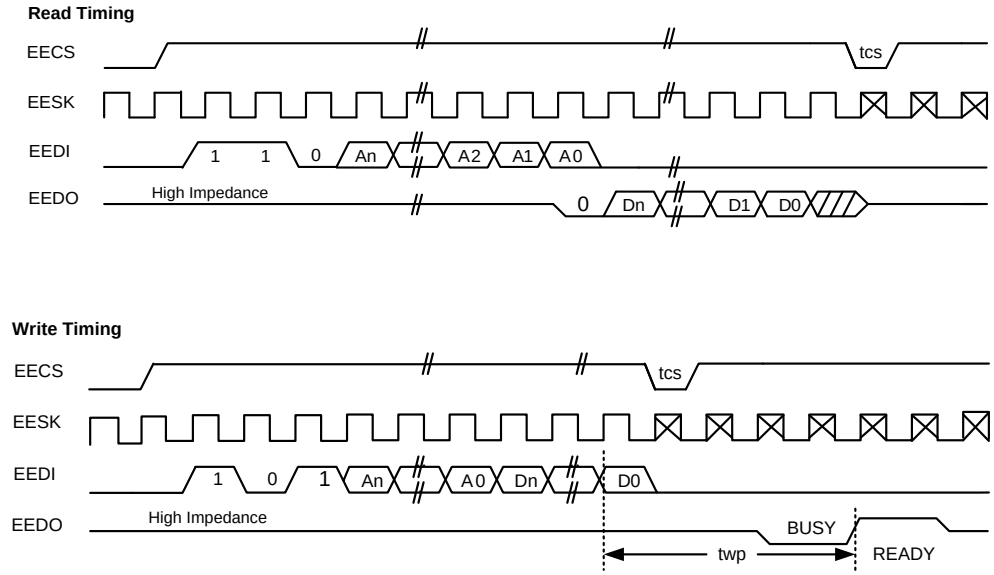


Figure 8. Serial EEPROM Interface Timing

Table 31. EEPROM Access Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
tcs	Minimum CS Low Time	4500	4600	4700	ns
tcss	CS Setup Time	494	504	514	ns
tcsh	CS Hold Time	-	0	-	ns
tskh	SK High Time	494	504	514	ns
tskl	SK Low Time	494	504	514	ns
tsk	SK Clock Cycle Time	988	1008	1028	ns
tdis	DI Setup Time	494	504	514	ns
tdih	DI Hold Time	494	504	514	ns
twp	Write Cycle Time	5.88	6	6.12	ms

10.10. PCI Express Bus Parameters

10.10.1. Differential Transmitter Parameters

Table 32. Differential Transmitter Parameters

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.800	-	1.05	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between The Jitter Median and Maximum Deviation from The Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note 1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.
Note 2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

10.10.2. Differential Receiver Parameters

Table 33. Differential Receiver Parameters

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	-	1.05	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between The Jitter Median and Maximum Deviation from The Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

10.10.3. REFCLK Parameters

Table 34. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-0.3	-	V	1, 8

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note 1: Measurement taken from single-ended waveform.

Note 2: Measurement taken from differential waveform.

Note 3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 12, page 42.

Note 4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 9, page 41.

Note 5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 9, page 41.

Note 6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 11, page 41.

Note 7: Defined as the maximum instantaneous voltage including overshoot. See Figure 9, page 41.

Note 8: Defined as the minimum instantaneous voltage including undershoot. See Figure 9, page 41.

Note 9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 9, page 41.

Note 10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note 11: System board compliance measurements must use the test load card described in Figure 15, page 43. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note 12: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100mV differential range. See Figure 14, page 42.

*Note 13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note 14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 10, page 41.

Note 15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

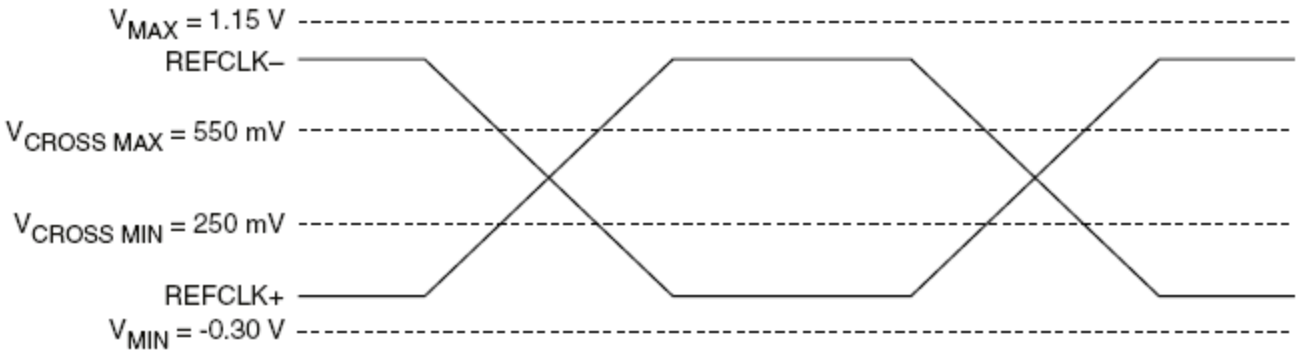


Figure 9. Single-Ended Measurement Points for Absolute Cross Point and Swing

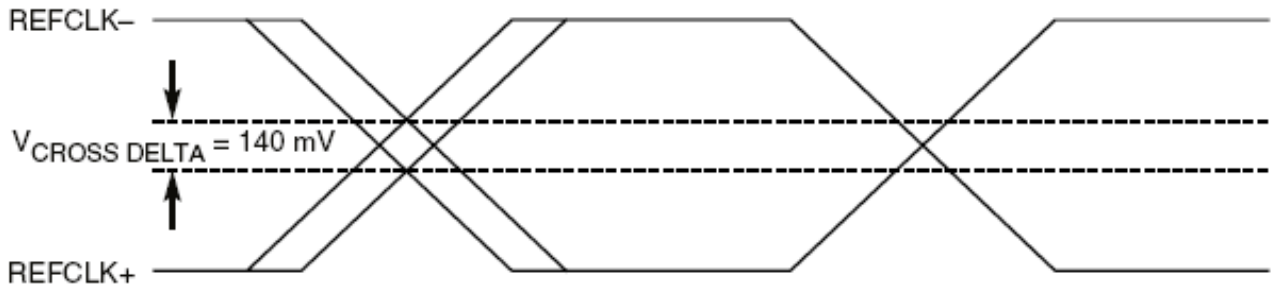


Figure 10. Single-Ended Measurement Points for Delta Cross Point

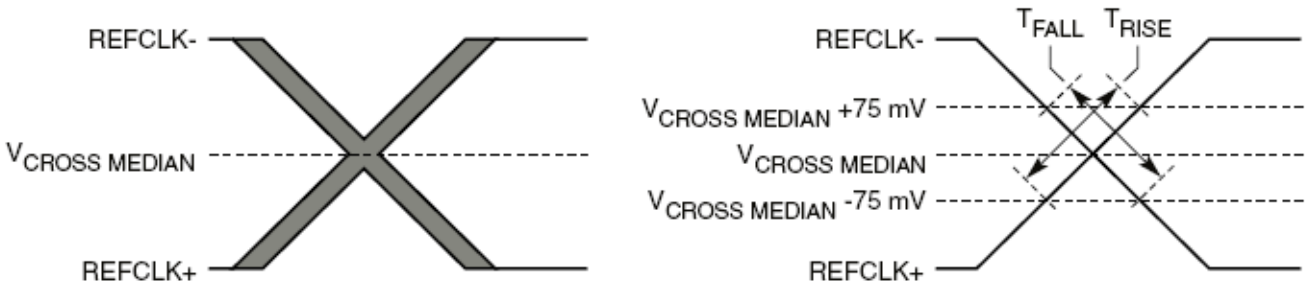


Figure 11. Single-Ended Measurement Points for Rise and Fall Time Matching

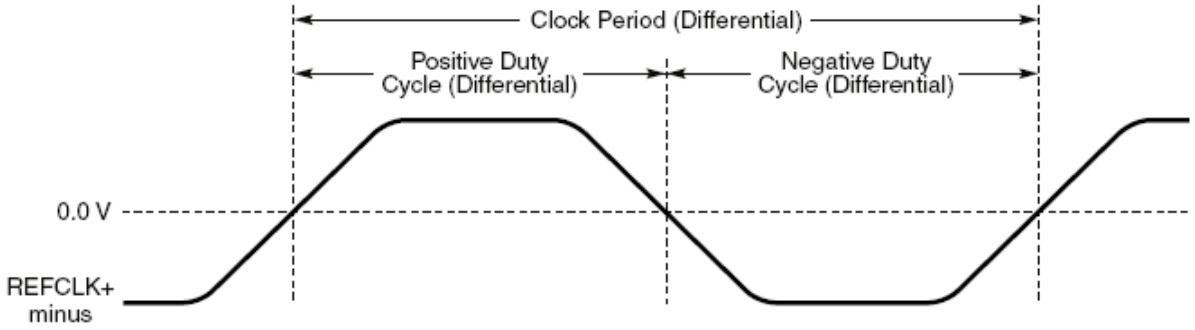


Figure 12. Differential Measurement Points for Duty Cycle and Period

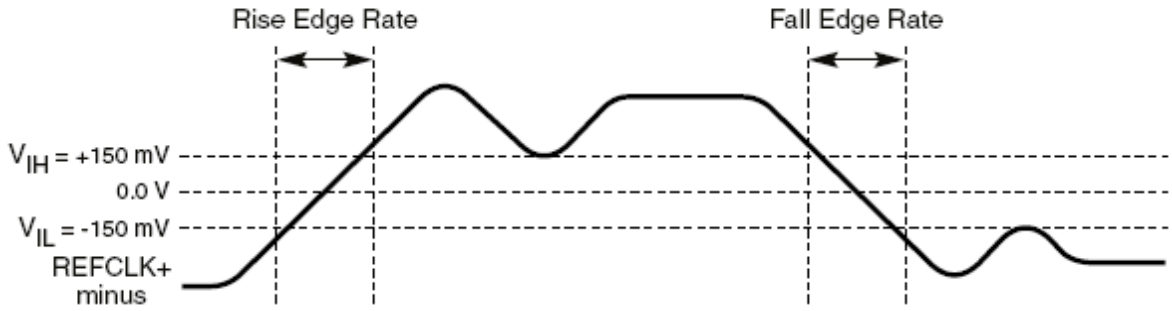


Figure 13. Differential Measurement Points for Rise and Fall Time

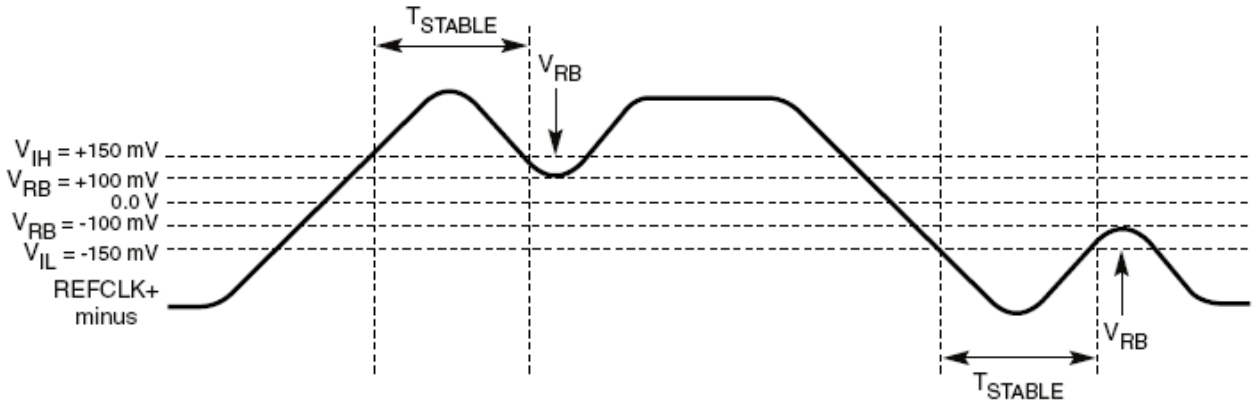


Figure 14. Differential Measurement Points for Ringback

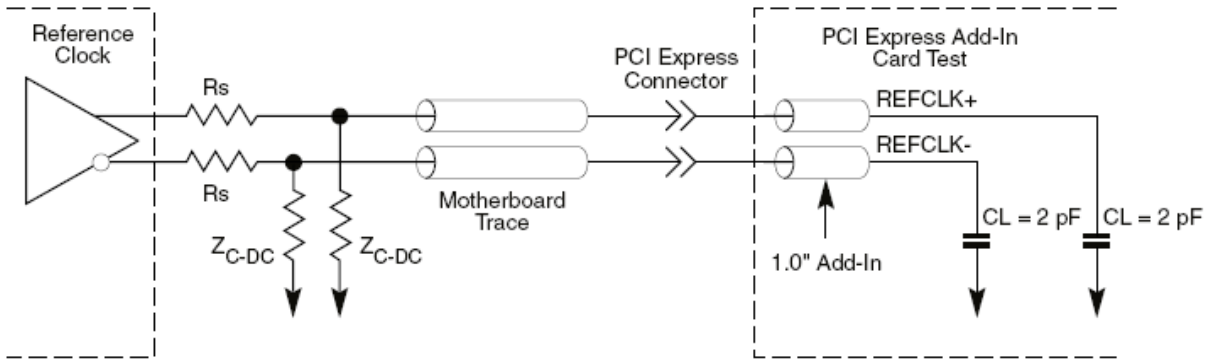


Figure 15. Reference Clock System Measurement Point and Loading

10.10.4. Auxiliary Signal Timing Parameters

Table 35. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
$T_{PERSTB-RTD}$	PERSTB Rising Time Duration	10	-	ms
T_{FAIL}*	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{PWRON}	3.3 Vaux Power On Time (Refer to Section 8, Page 31)	-	-	ms

Note 1: T_{FAIL} means 500 ns (maximum) from the power rail going out of specification (exceeding the specified tolerances by more than 500 mV). Refer to PCI Local Bus Specification rev. 3.0 for further information. T_{FAIL} can be disregarded when implementation and timing of T_{FAIL} will not affect any LAN functions.
Note 2: The ISOLATEB pin should follow the behavior of the 3.3V main power waveform.

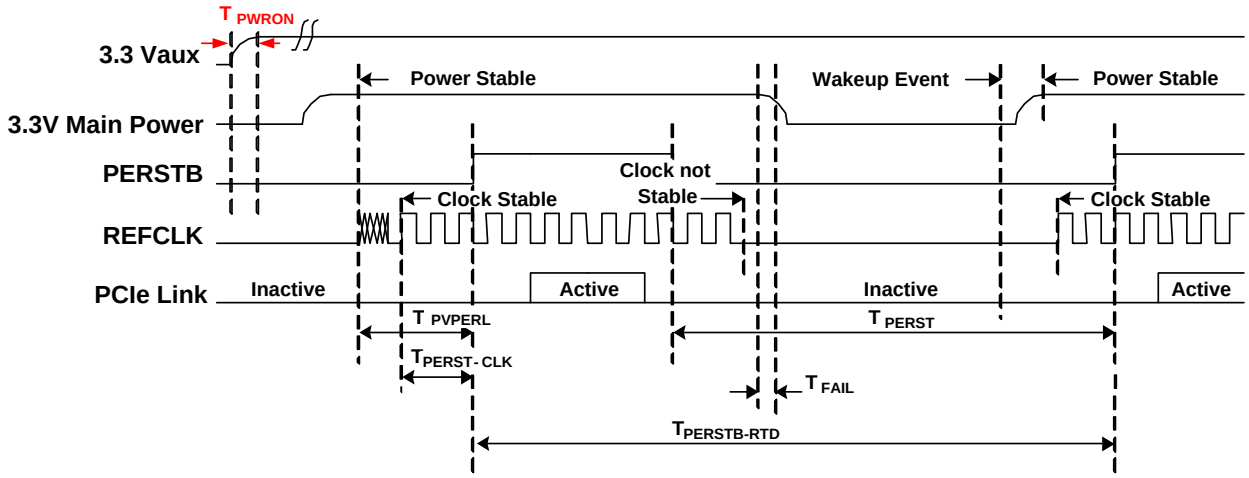


Figure 16. Auxiliary Signal Timing

10.11. Thermal Characteristics

Table 36. Thermal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
θ_{JA}	Junction-to-ambient thermal resistance $\theta_{JA} = (T_J - T_A)/P_H$	No air flow	-	19.06	-	°C/W
Ψ_{JT}	Junction-to-top-center thermal characterization parameter $\Psi_{JT} = (T_J - T_T)/P_H$	No air flow	-	0.28	-	°C/W

Note: T_J = junction temperature (°C), T_A = ambient temperature (°C), T_T = temperature on the top-center of the package (°C), P_H = total power dissipation (W).

The above thermal characteristics are based on customized PCB information, as shown in Table 37.

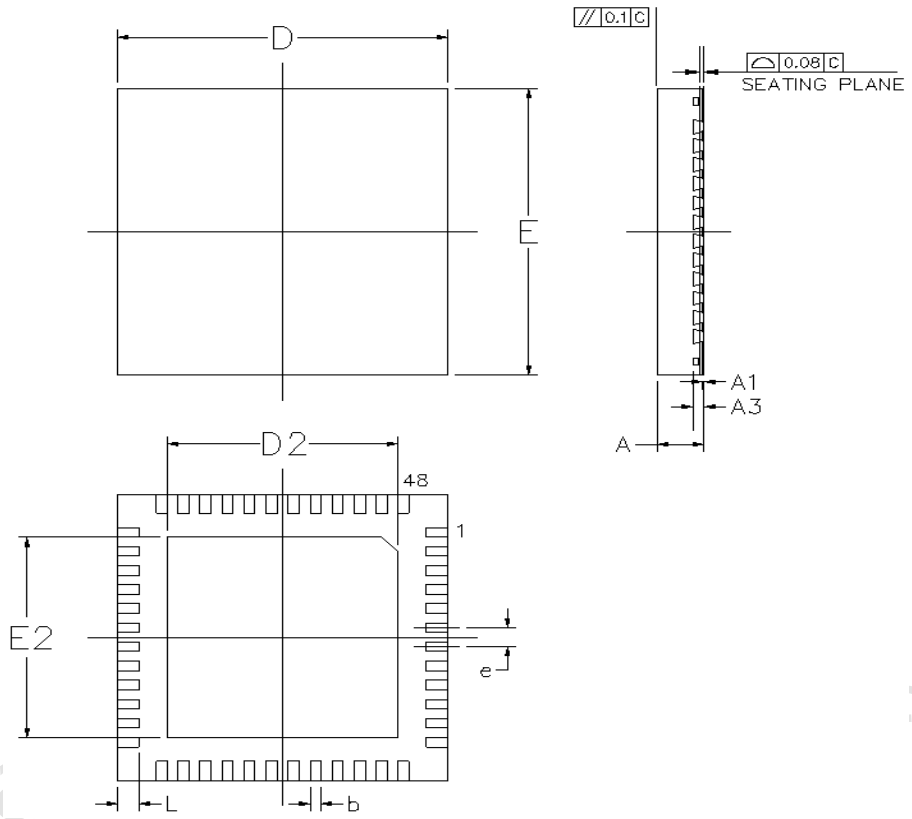
Table 37. PCB Information

PCB Type	Customized PCB
PCB Layers	4
PCB Dimensions	119.9 mm X 56 mm
Cu Coverage (%)	L1: 61% L2: 85% L3: 83% L4: 80%
External Heat Sink	No

Ψ_{JT} is better than θ_{JA} and θ_{JC} (Junction-to-case thermal resistance) for the estimation of the junction temperature (T_J). The temperature on the top-center of the package (T_T) is effected by not only the ambient temperature (T_A), but also the PCB conditions.

P_H includes the power dissipation from the top, bottom, and sides of the package, but θ_{JC} assumes that all the power is dissipated only from the top of the package. Thus, θ_{JC} is appropriate for the package attached with an external heat sink. In an actual environment, Ψ_{JT} brings a closer value to the actual T_J by measuringT_T.

11. Mechanical Dimensions



11.1. Mechanical Dimensions Notes

Table 38. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.750	0.850	1.000	0.030	0.034	0.039
A_1	0.000	0.020	0.050	0.000	0.001	0.002
A_3	0.200 REF			0.008 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
D/E	6.000BSC			0.236BSC		
D2/ E2	4.040	4.300	4.550	0.159	0.169	0.179
e	0.400BSC			0.016BSC		
L	0.300	0.400	0.500	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.
Note 3: The Max/Min for REF and BSC are +/- 0.1 MILLIMETER (mm).

12. Ordering Information

Table 39. Ordering Information

Part Number	Package	Status
RTL8125BG-CG	48-Pin QFN 'Green' Package	MP
RTL8125BGS-CG	48-Pin QFN 'Green' Package (with built-in switching regulator)	MP

Note: See pages 5(RTL8125BG) or page 6 (RTL8125BGS) for package identification information.

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